ROHINI
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Approved By AICTE & Affiliated to Anna University
NBA Accredited for All Eligible B.E/B.Tech Programs | NAAC Accredited with A+ Grade
Near Anjugramam - Kanyakumari Main Road, Palkulam, Variyoor P.O.-629401, Kanyakumari Dist, Tamil Nadu.

MINOR COURSE

VLSI- Design & Technology

Curriculum & Syllabus

(*2024-2025 Admitted Students Onwards*)

CREDIT INFO		
Sl.No	**Category**	**Credits**
1	**Minor Courses**	**18**

CREDIT DISTRIBUTION

Sl. No.	**Course Category**	**Credit/Semester**								**No. of Credits**
		I	**II**	**III**	**IV**	**V**	**VI**	**VII**	**VIII**	
1	MCC	**-**	**-**	**-**	**-**	**6**	**6**	**6**	**-**	**18**

VLSI- Design & Technology							
S. No.	Course Code	Course Title	Course Category	L	T	P	C
1	24VD501	Digital System Design with Verilog HDL	MCC	3	0	0	3
2	24VD502	CMOS VLSI Design and EDA Tools	MCC	3	0	0	3
3	24VD601	Physical Design, Verification and Design for Test	MCC	3	0	0	3
4	24VD602	Semiconductor Fabrication, Packaging and Reliability	MCC	3	0	0	3
5	24VD701	AI-Driven VLSI, Chiplet Architectures and Hardware Security	MCC	3	0	0	3
6	24VD702	Industry-Oriented Mini Project / Capstone Projects in VLSI design	MCC	0	0	6	3

Course Code:	24VD501	Course Title:	DIGITAL SYSTEM DESIGN WITH VERILOG HDL
Credits:	3	L – T – P	3-0-0
Pre-requisite			24EC302-Digital Logic Circuits and Design

Course objectives:

To impart knowledge on the

- Fundamentals of digital systems, digital design methodologies, and Hardware Description Languages (HDLs).
- Verilog HDL syntax, modeling techniques, simulation, synthesis, and RTL design concepts.
- Design and implementation of combinational and sequential digital circuits using Verilog HDL.
- Finite State Machine (FSM) design, verification methodologies, and digital system modeling using Verilog.
- FPGA-based digital design flow, synthesis concepts, and real-world applications of Verilog in embedded and digital systems.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Project based Learning
3. Experiential Learning
4. NPTEL and Other Videos
5. Smart Class Room
6. Flipped Class

UNIT I – INTRODUCTION TO DIGITAL SYSTEM DESIGN AND VERILOG	[9 hours]

Introduction to Digital System Design and Design Methodology– Design Abstraction Levels – ASIC and FPGA Overview – Register Transfer Level (RTL) Design Concepts – Introduction to Hardware Description Languages – Features of Verilog HDL – Structure of Verilog Modules – Module Ports and Port Mapping – Lexical Conventions – Data Types (Nets, Registers and Variables) – Constants – Operators – Compiler Directives – Continuous Assignments – Procedural Blocks – Blocking and Non-blocking Assignments

UNIT II – VERILOG MODELING OF COMBINATIONAL CIRCUITS	[9 hours]

Gate-Level, Dataflow, Behavioral and Structural Modeling – Hierarchical Design – RTL Design of Combinational Circuits– Design of Basic Logic Gates – Multiplexers – Demultiplexers – Encoders – Priority Encoders – Decoders – Comparators – Code Converters – Half Adder – Full Adder – Ripple Carry Adder – Carry Look-Ahead Adder – Arithmetic Logic Unit (ALU) – Parameterized Modules and Local Parameters – Generate Statements – RTL Coding Guidelines for Combinational Circuits – RTL Simulation – Synthesis Considerations.

UNIT III – VERILOG MODELING OF SEQUENTIAL CIRCUITS	[9 hours]

Sequential Logic Fundamentals – Latches – SR, JK, D and T Flip-Flops – Registers – Shift Registers – Ring and Johnson Counters – Synchronous and Asynchronous Counters – Up, Down and Up/Down Counters – Timing Parameters – Setup Time – Hold Time – Clock Skew – Propagation Delay – Edge-Triggered Sequential Modeling – Sequential Circuit Modeling using Verilog – Introduction to Verilog Memory Modeling.

UNIT IV – FINITE STATE MACHINES AND DIGITAL SYSTEM DESIGN	[9 hours]

Finite State Machine Concepts – Moore and Mealy Models – State Diagrams – State Tables – State Encoding Techniques (Binary and One-Hot Encoding) – FSM Modeling using Verilog – Sequence Detector – Traffic Light Controller – Vending Machine Controller – Controller–Datapath Design Concept – Test Bench Development – Clock and Reset Generation – Stimulus Generation - Test Bench-Based Functional Verification – Waveform Analysis – RTL Debugging Techniques.

UNIT V – RTL SYNTHESIS, VERIFICATION AND APPLICATIONS	[9 hours]

FPGA Design Flow (RTL Entry, Synthesis, Implementation, Place & Route, Bitstream Generation) – Technology Mapping – Timing Constraints and Timing Analysis – RTL Optimization - Resource Utilization – Introduction to SystemVerilog – Applications of Verilog in Digital Systems (UART Controller, PWM Generator, Memory Design and Simple Processor Datapath) – Embedded System Applications – Emerging Trends in HDL-Based Design (High-Level Synthesis and FPGA-Based AI Acceleration).

Course outcomes: On completion of the course, the student will have the ability to:

CO No	Course Outcomes	K Level
CO1	Explain the fundamentals of digital system design, Verilog HDL syntax, and digital design methodologies.	K2
CO2	Develop combinational logic circuits using different Verilog modeling techniques.	K3
CO3	Design sequential logic circuits and timing behavior using Verilog HDL.	K3
CO4	Develop and verify finite state machine (FSM) based digital systems using Verilog and simulation techniques.	K3
CO5	Apply synthesis concepts and FPGA design flow to implement Verilog-based digital systems for real-world applications.	K3

COs and POs Mapping:

COs	POs										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
CO1	3	2	1	–	–	–	–	–	–	–	1
CO2	2	3	3	–	2	–	–	–	1	–	1
CO3	2	3	3	–	2	–	–	–	1	–	1
CO4	3	2	3	–	2	–	–	–	1	–	1
CO5	3	2	3	2	2	–	–	–	1	–	1

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination	Theory Exam	100	60	60	60

(ESE)					
				Total	100

Assessment Pattern:

Bloom's Category	Continuous Assessment Tests		Terminal Examination
	1	2	
Remember	20	20	10
Understand	40	20	30
Apply	40	60	60
Analyze	0	0	0
Evaluate	0	0	0
Create	0	0	0

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions.
- All the fifteen questions have to be answered.

TEXT BOOKS

1. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Pearson Education, 2020. *(Units I–V)*
2. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, 4th Edition, McGraw-Hill Education, 2022. *(Units I–IV)*
3. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education, 2021. *(Units II–V)*
4. M. Morris Mano and Michael D. Ciletti, Digital Design, 6th Edition, Pearson Education, 2018. *(Units I–IV)*
5. Pong P. Chu, FPGA Prototyping by Verilog Examples, 2nd Edition, Wiley, 2023. *(Units IV–V)*

REFERENCE BOOKS

1. Zainalabedin Navabi, Verilog Digital System Design, 1st Edition, McGraw-Hill Education, 2006. (Units II, III, IV)
2. Charles H. Roth Jr. and Larry L. Kinney, Fundamentals of Logic Design, 8th Edition, Cengage Learning, 2021. (Units I, II, III)
3. Peter J. Ashenden, The Designer's Guide to Verilog HDL, 3rd Edition, Morgan Kaufmann (Elsevier), 2008. (Units I, II, III, IV)
4. Donald D. Givone, Digital Principles and Design, 1st Indian Reprint, McGraw-Hill Education, 2017. (Units I, II, III)
5. Shirshendu Roy, Advanced Digital System Design: A Practical Guide to Verilog Based FPGA and ASIC Implementation, 1st Edition, Springer Nature, 2024. (Units II, III, IV, V)
6. Pong P. Chu, FPGA Prototyping by Verilog Examples: Xilinx MicroBlaze MCS SoC Edition, 2nd Edition, Wiley, 2023. (Units IV, V)
7. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education, 2021. (Units II, III, IV, V)

WEB LINKS AND VIDEO LECTURES (E-RESOURCES)

1. https://nptel.ac.in/courses/117106114
2. https://nptel.ac.in/courses/106105165
3. https://hdlbits.01xz.net/wiki/Main_Page
4. https://onlinecourses.nptel.ac.in/e-learning/preview/noc24_cs61

SKILLED BASED ASSESSMENTS

1. Develop combinational circuits (MUX, Decoder, Encoder, Comparator) using Verilog.
2. Design an 8-bit Arithmetic Logic Unit (ALU) using Verilog HDL.
3. Implement synchronous and asynchronous counters using Verilog.
4. Design and verify a Universal Shift Register.
5. Develop a Sequence Detector using Moore/Mealy FSM.
6. Design a Traffic Light Controller using Verilog HDL.
7. Develop a Digital Clock or Stopwatch using FSM concepts.
8. Mini Project: Design and simulate a Verilog-based digital system such as a vending machine, elevator controller, UART controller, or simple processor datapath.

Course Code:	24VD502	Course Title:	CMOS VLSI Design and EDA Tools
Credits:	3	L – T – P	3-0-0
Pre-requisite			24EC302 DIGITAL LOGIC CIRCUITS AND DESIGN, 24VD501-DIGITAL SYSTEM DESIGN WITH VERILOG HDL

Course objectives:

To impart knowledge on the

- Fundamentals of CMOS technology, fabrication processes, and VLSI design methodology.
- CMOS logic design techniques, layout design principles, and physical design concepts.
- Design of combinational and sequential CMOS circuits with emphasis on power, delay, and area optimization.
- VLSI design automation using Electronic Design Automation (EDA) tools for schematic capture, simulation, layout, verification, and timing analysis.
- Application of CMOS VLSI design techniques and EDA tools for ASIC and System-on-Chip (SoC) design.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Project based Learning
3. Experiential Learning
4. NPTEL and Other Videos
5. Smart Class Room
6. Flipped Class

UNIT I – INTRODUCTION TO CMOS VLSI DESIGN	[9 hours]

Moore's Law – Design Hierarchy – Levels of Abstraction – VLSI Design Flow (ASIC and FPGA Overview) – Silicon Wafer Preparation and CMOS Fabrication Process– N-Well, P-Well and Twin-Tub Processes – Photolithography – Design Rules – Lambda-Based Design Rules – CMOS Scaling – Short Channel Effects – Process, Voltage and Temperature (PVT) Variations –Introduction to Standard Cell Design.

UNIT II – CMOS LOGIC DESIGN	[9 hours]
MOS Transistor Characteristics – CMOS Inverter – Voltage Transfer Characteristics – Noise Margins – Switching Characteristics – Propagation Delay – Power Dissipation in CMOS Circuits – Transistor Sizing and W/L Ratio – Static CMOS Logic – Dynamic CMOS Logic – Pass Transistor Logic – Transmission Gate Logic – Pseudo-NMOS Logic – Domino Logic – RC Delay Model and Elmore Delay – Logical Effort – Fan-in and Fan-out – Stick Diagrams – CMOS Layout Design Concepts.	

UNIT III – CMOS SUBSYSTEM DESIGN	[9 hours]
CMOS Implementation of Combinational Logic Circuits (NAND, NOR, XOR)– Arithmetic Circuits – Full Adder – Carry Look-Ahead Adder – Array Multiplier – Sequential Circuits – Latches – Flip-Flops – Registers – Timing Parameters of Sequential Circuits (Setup Time, Hold Time and Clock-to-Q Delay) – SRAM Cell – ROM Architecture – Interconnect Effects – RC Interconnect Model – Clock Distribution and Clock Skew – Pipelining Concepts – Low-Power CMOS Design Techniques.	

UNIT IV – EDA TOOLS AND PHYSICAL DESIGN	[9 hours]
Introduction to EDA Tools – RTL Design using HDL– Design Entry – Schematic Capture – Simulation and Functional Verification – Logic Synthesis – Timing Constraints and Synopsys Design Constraints (SDC) – Floor planning – Placement – Clock Tree Synthesis – Routing – Static Timing Analysis (STA) – Design Rule Checking (DRC) – Layout Versus Schematic (LVS) – Parasitic Extraction – Timing Optimization and Closure – Physical Verification and Design Sign-off.	

UNIT V – ASIC DESIGN FLOW AND APPLICATIONS	[9 hours]
RTL-to-GDSII ASIC Design Flow – Post Layout Verification – Design for Testability (DFT) – Scan Chains – Boundary Scan – Built-In Self-Test (BIST) – Power Analysis and Power Integrity – Signal Integrity – Reliability Issues (Electromigration, IR Drop and Electrostatic Discharge) – System-on-Chip (SoC) – Network-on-Chip (NoC) – Design for Manufacturability (DFM) – Emerging Trends in VLSI (AI Hardware Accelerators, Chiplet Technology and 3D ICs) – Applications of CMOS VLSI in Communication, Consumer Electronics, Automotive, Healthcare and IoT.	

Course outcomes: On completion of the course, the student will have the ability to:

CO No	Course Outcomes	K Level
CO1	Explain CMOS fabrication processes, VLSI design methodology, and CMOS technology fundamentals.	K2
CO2	Develop CMOS logic circuits and estimate their performance in terms of delay, power, and area.	K3
CO3	Develop CMOS combinational and sequential circuits using standard VLSI design principles.	K3
CO4	Apply EDA tools for schematic capture, simulation, synthesis, layout, and physical verification of CMOS VLSI circuits.	K3
CO5	Apply testing methodologies to obtain ASIC design flow, and develop modern VLSI applications using CMOS technologies.	K3

COs and POs Mapping:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	1	–	–	–	–	–	–	–	1
CO2	2	3	3	2	2	–	–	–	1	–	1
CO3	3	3	3	–	2	–	–	–	1	–	1
CO4	2	3	3	3	3	–	–	–	2	–	1
CO5	3	3	3	2	3	–	–	–	2	–	1

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			

End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

Assessment Pattern:

Bloom's Category	Continuous Assessment Tests		Terminal Examination
	1	2	
Remember	20	20	10
Understand	40	20	50
Apply	40	60	40
Analyze	0	0	0
Evaluate	0	0	0
Create	0	0	0

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions.
- All the fifteen questions have to be answered.

TEXT BOOKS

1. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 5th Edition, Pearson Education, 2015. (Units I–V)
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, 2003. (Units II–V)
3. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 4th Edition, McGraw-Hill Education, 2021. (Units I–V)
4. Wayne Wolf, Modern VLSI Design: IP-Based Design, 4th Edition, Pearson Education, 2008. (Units I, IV, V)

REFERENCE BOOKS

1. Kamran Eshraghian, Douglas A. Pucknell and Sholeh Eshraghian, Essentials of VLSI Circuits and Systems, 3rd Edition, PHI Learning, 2017.

2. Sabih H. Gerez, Algorithms for VLSI Design Automation, 2nd Edition, Wiley, 2006.
3. Michael John Sebastian Smith, Application-Specific Integrated Circuits (ASICs), 1st Edition, Pearson Education, 1997.
4. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education, 2021.
5. Bob Zeidman, Introduction to Verilog, 3rd Edition, Prentice Hall, 2014.
6. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, 5th Edition, Springer, 2013.

WEB LINKS AND VIDEO LECTURES (E-RESOURCES)

1. https://nptel.ac.in/courses/108107129
2. https://nptel.ac.in/courses/106105161
3. https://nptel.ac.in/courses/117106092
4. https://www.siemens.com/en-us/training/eda/

SKILLED BASED ASSESSMENTS

1. Analyze the voltage transfer characteristics and noise margins of a CMOS inverter.
2. Design CMOS layouts for basic logic gates using lambda-based design rules.
3. Estimate propagation delay and power consumption of CMOS combinational circuits.
4. Develop stick diagrams and layouts for arithmetic circuits such as full adders.
5. Perform schematic capture and functional simulation using an EDA tool.
6. Analyze timing reports and perform Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification.
7. Study and interpret an RTL-to-GDSII ASIC design flow using industry-standard EDA tools.
8. Mini Project: Design and analyze a CMOS-based subsystem (e.g., ALU, SRAM block, or arithmetic unit) and document the complete design flow from schematic to physical verification.

Course Code:	24VD601	Course Title:	Physical Design, Verification and Design for Test
Credits:	3	L – T – P	3-0-0
Pre-requisite			24VD502-CMOS VLSI Design and EDA Tools

Course objectives:

- To understand the VLSI physical design flow and learn to verify layouts using standard physical verification techniques.
- To implement DFT techniques for improving controllability, observability, and test coverage of digital systems.
- To apply timing, power, signal integrity, and reliability verification techniques for validating VLSI designs before fabrication.
- To apply BIST and Boundary Scan techniques for efficient testing of VLSI circuits.
- To explore and evaluate modern verification methodologies and industry-standard EDA tools for validating ASIC and SoC designs.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Project based Learning
3. Experiential Learning
4. NPTEL and Other Videos
5. Smart Class Room
6. Flipped Class

UNIT I – INTRODUCTION TO PHYSICAL DESIGN VERIFICATION	[9 hours]

Introduction to VLSI physical design flow - ASIC and SoC design flow - Physical design stages - Physical design verification - Design Rule Check (DRC) - Layout Versus Schematic (LVS) - Electrical Rule Check (ERC) - Antenna check - Density check - Process Design Kit (PDK) - Introduction to sign-off verification - Physical verification using EDA tools - Introduction to AI-assisted physical verification.

UNIT II – DESIGN FOR TESTABILITY	[9 hours]
Need for testing - Fault models (Stuck-at, Bridging, Transition and Delay Faults) - Controllability and Observability - Scan Cell Design - Full Scan and Partial Scan Techniques - Scan Chain Architecture - Automatic Test Pattern Generation (ATPG) - Fault Simulation - Fault Coverage - Test Compression -Embedded Deterministic Test (EDT) - Low-Power Testing Techniques - Design for Debug.	

UNIT III - PHYSICAL SIGN-OFF AND RELIABILITY VERIFICATION	[9 hours]
Static Timing Analysis (STA) - Clock tree verification - RC parasitic extraction - Signal integrity - Crosstalk analysis - Power integrity - IR drop analysis - Electromigration (EM) analysis - Electrostatic Discharge (ESD) verification - Latch-up analysis - Reliability verification - Introduction to process variation analysis - Thermal analysis - Sign-off methodology.	

UNIT IV - BUILT-IN SELF-TEST AND ADVANCED TEST TECHNIQUES	[9 hours]
Built-In Self-Test (BIST) - Logic BIST (LBIST) - Memory BIST (MBIST) - Linear Feedback Shift Register (LFSR) - Multiple Input Signature Register (MISR) - Test pattern generation - Output response compression - Boundary Scan (IEEE 1149.1) - IEEE 1500 embedded core testing - IEEE 1687 (IJTAG) - FPGA testing - High-Speed I/O testing - Introduction to silicon validation.	

UNIT V – MODERN VERIFICATION METHODOLOGIES AND EMERGING TRENDS	[9 hours]
Functional verification - Timing verification - Formal verification - Equivalence checking - Assertion-Based verification - Universal Verification Methodology (UVM) - Simulation-based verification - Hardware emulation and FPGA prototyping - Verification using AI and machine learning - Chiplet testing - 2.5D and 3D IC verification - Advanced packaging verification - RISC-V verification - Overview of industry EDA Tools (Cadence, Synopsys, Siemens EDA).	

TOTAL PERIODS : 45

Course outcomes: On completion of the course, the student will have the ability to:

CO No.	Course Outcomes	Cognitive Level
CO1	Understand the VLSI physical design flow and apply physical verification techniques to check layout correctness.	K2
CO2	Apply Design for Testability techniques, fault models, and scan-based testing	K3

	methods to improve the testability of digital circuits.	
CO3	Apply timing, power, signal integrity, and reliability verification techniques to validate VLSI designs.	K3
CO4	Apply Built-In Self-Test (BIST), Boundary Scan, and advanced testing techniques for efficient testing of VLSI circuits.	K3
CO5	Utilize modern verification methodologies and EDA tools for validating ASIC and SoC designs.	K3

COs and POs Mapping:

COs	**POs**										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
CO1	3	2	1	-	1	-	-	-	1	-	2
CO2	3	3	2	1	2	1	-	-	2	-	2
CO3	3	2	2	2	2	1	-	-	2	-	2
CO4	3	3	3	2	2	1	-	-	2	-	2
CO5	3	2	2	2	3	1	-	-	2	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	**Type of assessment**	**Max Marks**	**Reduced Marks**	**Total**	**Final marks**
Continuous Internal Examination (CIE) - Theory	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment – I	40	40		
	Skill Assessment – II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

Assessment Pattern:

Bloom's Category	Continuous Assessment Tests		Terminal Examination
	1	2	
Remember	20	20	20
Understand	40	40	40
Apply	40	40	40
Analyze	0	0	0
Evaluate	0	0	0
Create	0	0	0

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

TEXT BOOKS

1. M. L. Bushnell and V. D. Agrawal**,** Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2004.
2. Neil H. E. Weste and David Harris**,** CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson,2010
3. M. Abramovici, M. A. Breuer and A. D. Friedman**,** Digital Systems Testing and Testable Design, IEEE Press.

REFERENCE BOOKS

1. Chris Spear and Greg Tumbush**,** SystemVerilog for Verification, Springer.
2. Erik Seligman, Tom Schubert and M.V. Achutha Kiran Kumar**,** Formal Verification: An Essential Toolkit for Modern VLSI Design, Elsevier.
3. Jan M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits – A Design Perspective, Pearson.
4. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures: Design for Testability, 2006.

LINKS AND VIDEO LECTURES (E-RESOURCES):

- http://www.digimat.in/nptel/courses/video/106103116/L01.html
- http://www.digimat.in/nptel/courses/video/106103116/L02.html

- VLSI Physical Design https://youtu.be/lRpt1fCHd8Y?list=PLU8VFS-HdvKtKswbcvvA8yVhzleTV7OE8&t=22
- Testing of VLSI circuits https://youtu.be/lRf_UPXOnVU
- VLSI Physical Design with Timing Analysis https://youtu.be/H34hLpUU9PA?list=PLLy_2iUCG87Bny6CcGkCanvlHuXwr4-_W
- FPGA Based Signal Processing Systems

  https://youtu.be/e5G6pTXWNFo?list=PLLy_2iUCG87BbwCGLAQuGB2PeObWX64wT

SKILLED BASED ASSESSMENTS

1. Install KLayout **or** Magic VLSI and open a sample layout file. Observe the different layout layers and identify at least five layers used in CMOS layout.
2. Download and install any free VLSI layout viewer such as KLayout. Explore its basic menus and prepare a one-page report on the available verification features.
3. Design a simple AND-OR logic circuit using Logisim or any digital simulator. Inject a stuck-at fault and observe the change in the output.
4. Generate a truth table for a simple combinational circuit and manually identify the test vectors required to detect stuck-at faults. Compare the detected faults with the total number of possible faults.
5. Study a sample VLSI layout and identify possible crosstalk and routing congestion areas. Suggest simple methods to reduce these problems.
6. Measure the operating temperature of an FPGA or microcontroller board using a temperature sensor or datasheet values. Discuss how temperature affects chip reliability.
7. Develop a simple BIST block diagram for a 4-bit digital circuit using logic gates. Explain how the test patterns are generated and how faults are detected.
8. Design a 4-bit Linear Feedback Shift Register (LFSR) using Logisim or Verilog. Observe and record the pseudo-random output sequence.
9. Write and simulate a simple Verilog module (such as a Half Adder or Multiplexer) using EDA Playground or ModelSim. Verify the output using a testbench.
10. Compare the features of Cadence**,** Synopsys**,** and Siemens EDA tools by visiting their official websites. Prepare a comparison table highlighting their major verification applications.

Course Code:	24VD602	Course Title:	SEMICONDUCATOR FABRICATION, PACKING AND RELIABILITY
Credits:	3	L – T – P	3-0-0
Pre-requisite			24VD502-CMOS VLSI DESIGN AND EDA TOOLS 24VD601-PHYSICAL DESIGN, VERIFICATION AND DESIGN FOR TEST

Course objectives:

Students will be able to:

- To understand the fundamentals of semiconductor materials and crystal growth techniques.
- To study wafer preparation and cleaning processes used in IC fabrication.
- To learn various oxidation, diffusion, and ion implantation techniques.
- To understand lithography, etching, and thin film deposition processes.
- To gain knowledge about advanced fabrication techniques and packaging.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. PowerPoint presentation
3. Interactive Simulations
4. Lab experiment videos
5. Blended Mode of Learning
6. Project based Learning
7. Experiential Learning
8. NPTEL and Other Videos
9. Smart Class Room
10. Flipped Class

UNIT I SEMICONDUCTOR MATERIALS & CRYSTAL GROWTH	9 hours
Semiconductor basics: Intrinsic and extrinsic semiconductors, Silicon crystal structure and properties Crystal growth techniques: Czochralski (CZ) method, Float Zone method, Wafer slicing, polishing, and epitaxy, Introduction to compound semiconductors.	
UNIT II WAFER PREPARATION & CLEANING	**9 hours**

Wafer preparation steps, Surface cleaning techniques: RCA cleaning process, Chemical and mechanical polishing (CMP), Defects in wafers and their control, Cleanroom technology and contamination control.	
UNIT III OXIDATION, DIFFUSION & ION IMPLANTATION	**9 hours**
Thermal oxidation: Dry and wet oxidation, Oxide growth kinetics, Diffusion process: Fick's laws Ion implantation: Principles and equipment, Annealing process.	
UNIT IV LITHOGRAPHY & ETCHING	**9 hours**
Photolithography process: Steps and equipment, Photoresists: Types and properties, Mask alignment and exposure techniques, Etching: Wet etching and dry etching (plasma etching), Pattern transfer techniques.	
UNIT V – THIN FILM DEPOSITION & PACKAGING	**9 hours**
Thin film deposition: CVD, PVD, sputtering, Metallization techniques, Dielectric film deposition IC packaging methods, Introduction to VLSI fabrication and advanced technologies.	
Total: 45 hours	

Course outcomes:

On completion of the course, the student will have the ability to:

COs	Course Outcomes	Cognitive Level
CO1	Explain semiconductor materials and crystal growth methods.	**K2**
CO2	Describe wafer preparation and cleaning techniques.	**K2**
CO3	Analyze oxidation, diffusion, and ion implantation processes.	**K3**
CO4	Understand lithography and etching techniques used in IC fabrication.	**K2**
CO5	Apply knowledge of thin film deposition and packaging in semiconductor manufacturing.	**K3**

COs and POs Mapping:

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	3	2	2	2	1	-	-	-	1	-	-	2
CO2	3	2	2	2	2	-	-	-	1	-	-	2
CO3	3	2	2	2	2	-	-	-	1	-	-	2
CO4	3	2	2	2	2	-	-	-	1	-	-	2
CO5	3	3	3	3	2	-	-	-	1	-	-	2

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	**Type of assessment**	**Max Marks**	**Reduced Marks**	**Total**	**Final marks**
Continuous Internal Examination (CIE)	CIE – I	100	50	100	40
	CIE – II	100			
	MCQ	20	10		
	Skill Assessment - I	40	40		
	Skill Assessment - II	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
				Total	100

End semester Examination: (QP PATTERN)

- Each unit consists of two 2 marks questions and one 16 marks question (either or).
- All the fifteen questions have to be answered.

Assessment Pattern:

Bloom's Category	Continuous Assessment Tests		Terminal Examination
	1	2	
Remember	20	20	20
Understand	80	60	60
Apply	0	20	20
Analyze	0	0	0
Evaluate	0	0	0
Create	0	0	0

TEXT BOOKS:

1. S. M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley.
2. Peter Van Zant, Microchip Fabrication: A Practical Guide, McGraw-Hill.
3. Gary S. May & Simon M. Sze, Fundamentals of Semiconductor Fabrication, Wiley.

REFERENCES

1. S. M. Sze & Kwok K. Ng – Physics of Semiconductor Devices
2. Gary S. May & Simon M. Sze – Fundamentals of Semiconductor Fabrication
3. Peter Van Zant – Microchip Fabrication

Web Links and Video Lectures (E-Resources):

1. https://www.youtube.com/watch?v=bor0qLifjz4
2. https://www.youtube.com/watch?v=NGFhc8R_uO4

Online Courses:

1. **https://www.youtube.com/watch?v=CE7yVSu5MPs**

Suggested Skill Activities:

1. Demonstrate cleanroom safety and gowning procedure.
2. Practice safe silicon wafer handling techniques.
3. Simulate crystal growth using CZ method software.
4. Study RCA wafer cleaning process steps.
5. Analyse dry vs wet oxidation processes.
6. Prepare photolithography process flow diagram.
7. Design a basic IC layout using CAD tools.

8. Compare wet and dry etching methods.
9. Present CVD, PVD, and sputtering techniques.
10. Develop a simple MOSFET fabrication flow.

Course Code:	24VD701	Course Title:	AI-Driven VLSI, Chipset Architectures and Hardware Security
Credits	3	L – T – P	3-0-0
Pre-requisite	24VD502-CMOS VLSI DESIGN AND EDA TOOLS 24VD601-PHYSICAL DESIGN, VERIFICATION AND DESIGN FOR TEST		

Course Objective

To impart knowledge on the

- AI-assisted VLSI design methodologies and Electronic Design Automation (EDA).
- Modern chipset architectures for AI and heterogeneous computing.
- Hardware security principles and secure integrated circuit design.
- AI applications in VLSI verification, testing, and optimization.
- Emerging trends in secure AI hardware and semiconductor technologies.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

1. Chalk and Talk
2. Case Studies
3. EDA Tool Demonstrations
4. AI-enabled Simulation and Design Exercises
5. Industry-Oriented Mini Projects
6. Flipped Classroom
7. Multimedia and Online Learning Resources

UNIT I AI IN VLSI DESIGN AUTOMATION	9 Hours
Introduction to AI in semiconductor design, Machine Learning for Electronic Design Automation (EDA), AI-assisted logic synthesis, floor-planning, placement and routing, power and timing optimization, AI-driven analog circuit design, design space exploration, reinforcement learning in chip design.	
UNIT II MODERN CHIPSET ARCHITECTURES	**9 Hours**

Evolution of processor architectures, Chiplet-based architectures, System-on-Chip (SoC), Network-on-Chip (NoC), AI accelerators, GPU, TPU and NPU architectures, heterogeneous computing, memory hierarchy, interconnect technologies, advanced packaging techniques.	
UNIT III AI-DRIVEN VERIFICATION AND TESTING	**9 Hours**
Functional verification using AI, intelligent test pattern generation, fault diagnosis using Machine Learning, design-for-testability (DFT), built-in self-test (BIST), yield prediction, predictive maintenance in semiconductor manufacturing, reliability analysis.	
UNIT IV HARDWARE SECURITY	**9 Hours**
Hardware security fundamentals, hardware Trojans, side-channel attacks, fault injection attacks, physically unclonable functions (PUFs), secure boot, hardware root of trust, cryptographic hardware accelerators, secure IC design methodologies, trusted semiconductor manufacturing.	
UNIT V EMERGING TRENDS IN AI HARDWARE	**9 Hours**
Neuromorphic computing, quantum-aware chip architectures, RISC-V based AI processors, edge AI hardware, Tiny ML processors, AI-enabled cyber-physical systems, secure AI hardware, sustainability in semiconductor manufacturing, future semiconductor technologies.	

Course outcomes:

On completion of the course, the student will have the ability to:

CO No.	Course Outcomes	Cognitive Level
CO1	Explain AI techniques used in VLSI design automation.	K2
CO2	Analyze modern chipset architectures for AI computing applications.	K4
CO3	Apply AI methods for VLSI verification and testing.	K3
CO4	Evaluate hardware security threats and secure IC design techniques.	K2
CO5	Design secure AI-enabled semiconductor systems considering emerging technologies.	K5

COs and POs Mapping:

COs	POs										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
CO1	3	2	2	1	3	-	-	-	-	-	2

CO2	3	3	2	2	3	-	-	-	-	-	2
CO3	3	3	3	3	3	-	-	1	-	-	2
CO4	3	3	2	3	3	1	2	1	-	-	2
CO5	3	3	3	3	3	1	2	2	1	2	3

Scheme of Evaluation

Component	**Type of assessment**	**Max Marks**	**Reduced Marks**	Total	Final Marks
Continuous Internal Examination (CIE) – Theory	CIE - 1	100	50	100	40
	CIE - 2	100			
	MCQ	20	10		
	Skill Assesment - 1	40	40		
	Skill Assesment - 2	40			
End Semester Examination (ESE)	Theory Exam	100	60	60	60
Total					100

End semester Examination: (QP PATTERN)

• Each unit consists of two 2 marks questions and one 16 marks question (either or).

• All the fifteen questions have to be answered.

Assessment Pattern:

Bloom's Category	**Continuous Assessment Tests**		**Terminal Examination**
	1	**2**	

Remember	10	10	10
Understand	20	20	20
Apply	70	70	70
Analyze	0	0	0
Evaluate	0	0	0
Create	0	0	0

Text Books:

1. Michael Keating et al., Reuse Methodology Manual for System-on-Chip Design, Springer, Latest Edition.
2. Wayne Wolf, Modern VLSI Design: IP-Based Design, Pearson.
3. Rajat Subhra Chakraborty and Swarup Bhunia, Hardware Security: Design, Threats and Safeguards, CRC Press.
4. Cem Unsalan, Bora Tar and H. Deniz Gurhan, Digital System Design with FPGA: AI and Hardware Applications, McGraw Hill**.**

Reference Books

1. Neil Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson.
2. Jan Rabaey, Digital Integrated Circuits, Pearson.
3. Swarup Bhunia and Mark Tehranipoor, Hardware Security: A Hands-on Learning Approach, Morgan Kaufmann.
4. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer.
5. Hennessy and Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann.

Web Links and Video Lectures (E-Resources):

1. NPTEL – VLSI Design Courses: https://nptel.ac.in
2. Cadence Learning Portal: https://www.cadence.com
3. Synopsys Learning Center: https://www.synopsys.com
4. RISC-V International: https://riscv.org
5. IEEE Hardware Security Resources: https://ieeexplore.ieee.org

Online Courses:

1. NPTEL – VLSI Design
2. NPTEL – Hardware Security
3. Coursera – AI for Chip Design
4. edX – Computer Architecture
5. SWAYAM – Semiconductor and VLSI Courses

Suggested Skill Activities:

1. Implement AI-assisted placement and routing using open-source EDA tools.
2. Design and simulate a simple AI accelerator on FPGA.
3. Analyze power, timing and area optimization using AI-based techniques.
4. Develop a System-on-Chip architecture for an embedded AI application.
5. Detect hardware Trojans using machine learning algorithms.
6. Design and implement a Physically Unclonable Function (PUF).
7. Perform side-channel attack analysis on cryptographic hardware.
8. Compare GPU, TPU, NPU and RISC-V AI processor architectures.
9. Build a secure AI-enabled edge computing prototype.
10. Study recent semiconductor technologies and prepare a case study on AI-driven chip design.

Course Code:	24VD702	Course Title:	INDUSTRY ORIENTED MINI PROJECT/CAPSTONE PROJECTS IN VLSI DESIGN
Credits:	3	L – T – P	3-0-0
Pre-requisite			24VD701-AI-Driven VLSI, Chipset Architectures and Hardware Security

Course objectives:

The course enables the students to:

1. Identify and analyze real-world problems in semiconductor, VLSI, and embedded system industries suitable for innovative hardware design solutions.
2. Apply VLSI design methodologies, EDA tools, and project management techniques to develop industry-oriented integrated circuit solutions.
3. Design, simulate, verify, and implement digital, analog, mixed-signal, or FPGA-based systems using modern VLSI design tools.
4. Evaluate VLSI designs with respect to performance, power consumption, area, reliability, manufacturability, and scalability.
5. Demonstrate professional, ethical, teamwork, entrepreneurship, and lifelong learning skills through successful completion and presentation of a VLSI design project.

Teaching-Learning Process:

Suggested strategies that teachers may use to effectively achieve the course outcomes:

- Design Thinking Workshops
- Industry Mentoring Sessions
- Agile Development Methodology
- Collaborative Team Learning
- Hands-on Development using IoT Hardware and Cloud Platforms
- Simulation and Prototype Development
- Technical Design Reviews
- Project Demonstrations
- Viva Voce and Technical Presentations

UNIT I - PROJECT IDENTIFICATION, REQUIREMENT ANALYSIS AND PLANNING	[9 hours]
Semiconductor Industry Trends and Challenges – VLSI Product Development Lifecycle – Problem Identification and Project Selection – Industry Requirements and Specifications – Design Thinking and Innovation – Literature Survey and Patent Search – Requirement Analysis – Functional and Non-Functional Specifications – Feasibility Analysis – Project Planning – Risk Assessment – Design Flow Selection.	
UNIT II – VLSI SYSTEM DESIGN AND ARCHITECTURE DEVELOPMENT	**[9 hours]**
VLSI Design Methodology – System-Level Modeling – RTL Architecture Design – ASIC and FPGA Design Flows – IP Core Selection and Reuse – Hardware-Software Co-Design Concepts – Memory and Interface Design – Low-Power Design Considerations – Design Constraints – Architecture Validation and Prototype Planning.	
UNIT III – IMPLEMENTATION, SIMULATION AND VERIFICATION	**[9 hours]**
HDL-Based Design Using Verilog/VHDL/SystemVerilog – Functional Simulation – FPGA Prototyping – Synthesis and Optimization – Timing Analysis – Testbench Development – Functional Verification – Power and Area Estimation – Debugging Techniques – Design Documentation.	
UNIT IV – PHYSICAL DESIGN, TESTING AND ENTREPRENEURSHIP	**[9 hours]**
Floor Planning – Placement and Routing Concepts – Clock Tree Synthesis – Static Timing Analysis – Design Rule Checking (DRC) – Layout Versus Schematic (LVS) Verification – Design for Testability (DFT) Concepts – Reliability and Yield Considerations – Intellectual Property Rights (IPR) – Semiconductor Startups and Entrepreneurship Opportunities.	
UNIT V – INDUSTRIAL APPLICATIONS, CASE STUDIES AND PROJECT DEMONSTRATION	**[9 hours]**
VLSI Applications in Consumer Electronics – Communication Systems and 5G Hardware – AI Accelerators and Edge Computing Hardware – Automotive Electronics and ADAS Systems – IoT and Wearable Devices – Biomedical VLSI Systems – High-Speed and Low-Power Processor Design – FPGA-Based Industrial Solutions – Semiconductor Industry Case Studies – Final Project Demonstration.	

Total Period:45

Course outcomes:

On completion of the course, the student will have the ability to:

CO	Course Outcomes	Cognitive Level
CO1	Identify and analyse real-world engineering problems suitable for VLSI-based solutions.	K4
CO2	Design and develop digital, analog, or FPGA-based systems using modern VLSI design methodologies and EDA tools.	K3
CO3	Integrate verification, optimization, and implementation techniques to enhance VLSI system performance.	K4
CO4	Evaluate VLSI designs based on power, area, speed, reliability, manufacturability, and industrial applicability.	K5
CO5	Demonstrate a professionally developed VLSI solution with complete technical documentation, validation, and presentation.	K3

COs and POs Mapping:

COs	POs										
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO1	**3**	**3**	**3**	**1**	**3**	**-**	**-**	**2**	**1**	**2**	**1**
CO2	**3**	**3**	**3**	**1**	**3**	**-**	**1**	**2**	**1**	**2**	**1**
CO3	**3**	**3**	**3**	**2**	**3**	**-**	**-**	**2**	**1**	**2**	**1**
CO4	**2**	**3**	**3**	**2**	**3**	**-**	**-**	**2**	**2**	**2**	**2**
CO5	**3**	**3**	**3**	**2**	**3**	**-**	**-**	**2**	**1**	**3**	**1**

Level 3- Highly Mapped, Level 2- Moderately Mapped, Level 1- Low Mapped, Level 0- Not Mapped

Scheme of Evaluation:

Component	Type of assessment	Max Marks	Reduced Marks	Total	Final marks
Continuous Internal Assessment	Evaluation of Different modules of work and Report	100	75	100	100
End Semester Examination (ESE)	Exam	100	25		
Total					100

TEXT BOOKS

1. Harry Veendrick, Nanometer CMOS ICs: From Basics to ASICs, 3rd Edition, Springer Cham, 2024, ISBN: 978-3031642487.
2. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson.
3. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson, 5th Edition, 2019.
4. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson, 3rd Edition, 2021.

REFERENCE BOOKS

1. Koushik Guha et al. (Eds.), Exploring the Intricacies of Digital and Analog VLSI, IGI Global Scientific Publishing, 2025, ISBN: 979-8369380840.
2. P. Brundavani et al., An Introduction to VLSI Design and Testing, Garuda Publishers, 2025.
3. Soumitra R. Joy and Pinaki Mazumder, Artificial Plasmonics for VLSI Interconnects, Wiley, 2025, ISBN: 978-1394289950.
4. David Money Harris and Sarah Harris, Digital Design and Computer Architecture, Morgan Kaufmann, 2021.
5. Pong P. Chu, FPGA Prototyping by Verilog Examples, Wiley, Latest Edition.

WebLinks and Video Lectures (E-Resources):

1. https://www.youtube.com/@RTL2GDSII
2. https://www.youtube.com/watch?v=AhiQeP002ZU
3. https://www.youtube.com/@TeamVLSI

Online Courses:

1. https://nptel.ac.in/courses/117106092
2. https://www.maven-silicon.com/vlsi/free-vlsi-training-courses/

Suggested Skill Activities:

Students shall complete the following project-oriented activities.

1. Identify an industry-relevant VLSI design problem.
2. Prepare project proposal and design specifications.
3. Perform RTL design using Verilog/VHDL.
4. Develop simulation and verification environments.
5. Implement FPGA-based prototypes.
6. Perform synthesis and timing analysis.
7. Optimize power, area, and speed metrics.
8. Conduct functional and performance verification.
9. Prepare technical reports and design documentation.
10. Demonstrate the final design through simulation, FPGA implementation, or ASIC design flow.

Suggested Capstone Project Domains

- Low-Power Arithmetic Logic Unit (ALU)
- RISC-V Processor Design
- FPGA-Based Digital Signal Processor
- AI Accelerator for Edge Devices
- CNN Hardware Accelerator
- Network-on-Chip (NoC) Design
- High-Speed UART Controller
- SPI/I2C Communication Controller
- Low-Power SRAM Design

- Cache Memory Controller
- AES Encryption Hardware
- FPGA-Based Image Processing System
- Traffic Light Controller on FPGA
- Digital Clock and Timer System
- Smart Energy Meter Interface Controller
- Hardware Trojan Detection System
- IoT Sensor Interface SoC
- Biomedical Signal Processing Hardware
- FPGA-Based Motor Control System
- ASIC Design of Digital Filters