

UNIT III

IO INTERFACING

Interfacing

Interface is the path for communication between two components. Interfacing is of two types, memory interfacing and I/O interfacing.

Memory Interfacing

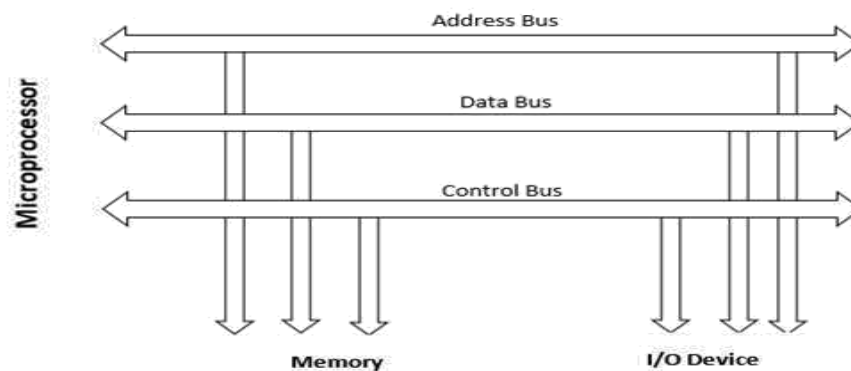
When we are executing any instruction, we need the microprocessor to access the memory for reading instruction codes and the data stored in the memory. For this, both the memory and the microprocessor requires some signals to read from and write to registers.

The interfacing process includes some key factors to match with the memory requirements and microprocessor signals. The interfacing circuit therefore should be designed in such a way that it matches the memory signal requirements with the signals of the microprocessor.

IO Interfacing

There are various communication devices like the keyboard, mouse, printer, etc. So, we need to interface the keyboard and other devices with the microprocessor by using latches and buffers. This type of interfacing is known as I/O interfacing.

Block Diagram of Memory and I/O Interfacing



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Few interfacing chips 8086

- Memory Interfacing & I/O interfacing
- Parallel communication interface {8255 PPI}
- Serial communication interface {8251 USART}
- D/A and A/D Interface {ADC 0800/0809, DAC0800}
- Timer {or counter} {8253/8254 Timer}
- Keyboard /display controller {8279}
- Interrupt controller {8259}
- DMA controller {8237/8257}

PARALLEL COMMUNICATION INTERFACE: 8255 (PROGRAMMABLE PERIPHERAL INTERFACE AND INTERFACING)

The 8255 is a widely used, programmable parallel I/O device. It can be programmed to transfer data under data under various conditions, from simple I/O to interrupt I/O. It is an important general purpose I/O device that can be used with almost any microprocessor.

The 8255 has **24 I/O pins** that can be grouped primarily into two 8 bit parallel **ports: A and B**, with the remaining 8 bits as **Port C**. The 8 bits of port C can be used as individual bits or be grouped into two 4 bit ports: **CUpper (CU) and CLower (CL)**. The functions of these ports are defined by writing a control word in the control register.

8255 can be used in two modes: **Bit set/Reset (BSR) mode and I/O mode**.

- The BSR mode is used to set or reset the bits in port C.
- The I/O mode is further divided into 3 modes:
 - mode 0- all ports function as simple I/O ports
 - mode 1 - a handshake mode whereby Port A and/or Port B use bits from Port C as handshake signals
 - mode 2- Port A can be set up for bidirectional data transfer using handshake signals from Port C, and Port B can be set up either in mode 0 or mode 1.

PIN DETAILS

PA3	1		40	PA4
PA2	2		39	PA5
PA1	3		38	PA6
PA0	4		37	PA7
RD	5		36	WR
CS	6		35	RESET
gnd	7		34	D0
A1	8		33	D1
A0	9		32	D2
PC7	10	8255	31	D3
PC6	11	PPI	30	D4
PC5	12		29	D5
PC4	13		28	D6
PC0	14		27	D7
PC1	15		26	Vcc
PC2	16		25	PB7
PC3	17		24	PB6
PB0	18		23	PB5
PB1	19		22	PB4
PB2	20		21	PB3

Pins of 8255

The signal description of 8255 is briefly presented as follows:

PA7-PA0: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.

PC7-PC4: Upper nibble of port C lines. They may act as either output latches or input buffers lines. This port also can be used for generation of handshake lines in mode 1 or mode 2.

PC3-PC0: These are the lower port C lines, other details are the same as PC7-PC4 lines.

PB0-PB7: These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.

RD: This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.

WR: This is an input line driven by the microprocessor. A low on this line indicates write operation.

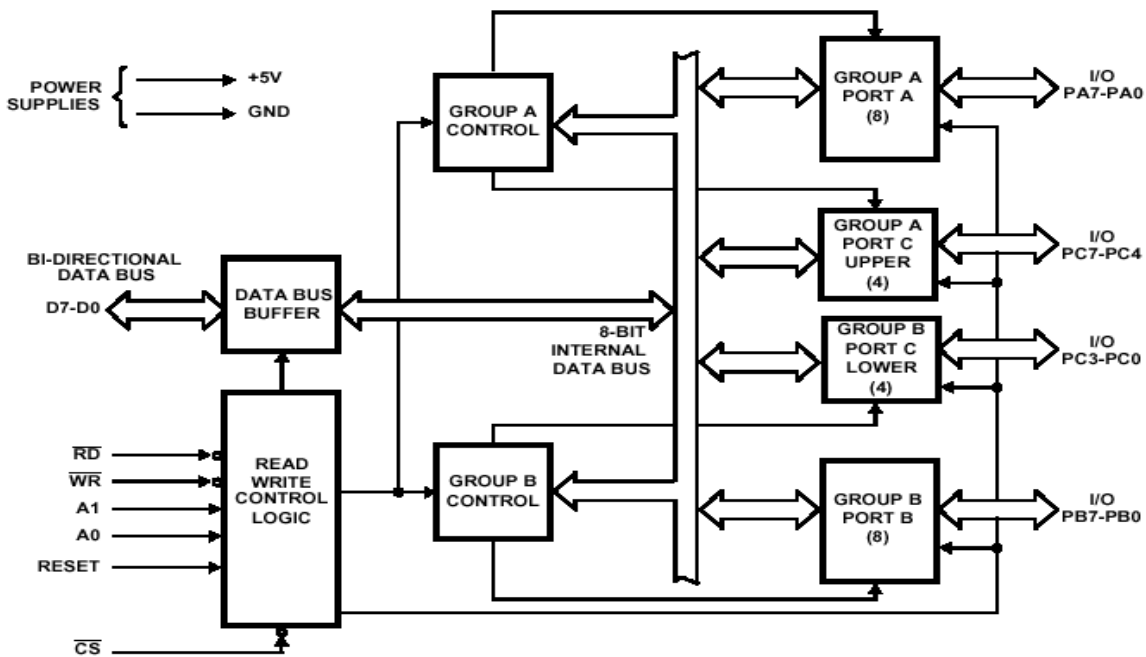
CS: This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.

A1-A0: These are the address input lines and are driven by the microprocessor. These lines A1-A0 with RD, WR and CS from the following operations for 8255. In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the A0 and A1 pins of 8255 are connected with A1 and A2 respectively.

D0-D7: These are the data bus lines those carry data or control word to/from the microprocessor.

RESET: A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

8255 Block Diagram:



Block Diagram of the 8255 Programmable Peripheral Interface (PPI)

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Data Bus Buffer-This three-state bi-directional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

- **(CS)** Chip Select. A "low" on this input pin enables the communication between the 8255 and the CPU.
- **(RD)** Read. A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.
- **(WR)** Write. A "low" on this input pin enables the CPU to write data or control words into the 8255.
- **(A0 and A1)** Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).
- **(RESET)** Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode.

A1	A0	SELECTION
0	0	PORT A
0	1	PORT B
1	0	PORT C
1	1	CONTROL

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Ports A, B, and C

The 8255 contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

- **Port A** One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-

- down" bus-hold devices are present on Port A.
- **Port B** One 8-bit data input/output latch/buffer and one 8-bit data input buffer.
- **Port C** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B.

Operation modes of 8255:

The bit pattern loaded in control word register specifies an I/O function for each port and the mode of operation in which the ports are to be used.

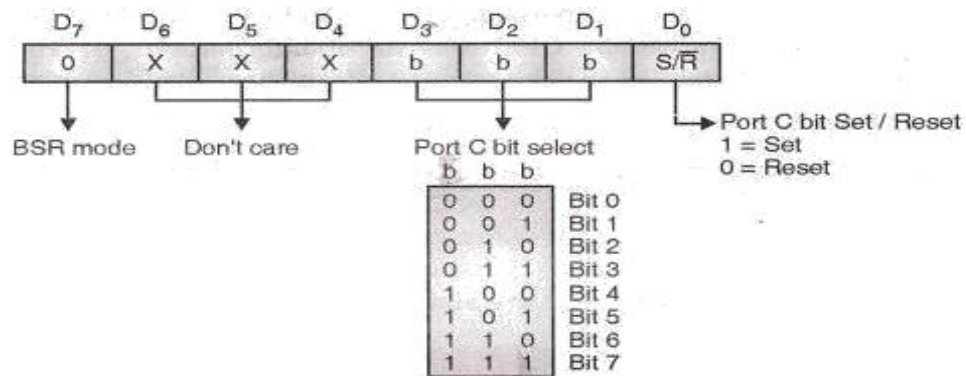
There are two different control word formats which specify two basic modes:

- BSR (Bit set reset)mode
- I/O mode

The two basic modes are selected by $D7$ bit of control register. When $D7=1$ it is an I/O mode and when $D7=0$; it is a BSR mode.

BSR mode-

1. The BSR mode is a port C bit set/resetmode.
2. The individual bit of port C can be set or reset by writing control word in the controlregister.
3. The control word format of BSR mode is as shown in the figurebelow



BSR control word format

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

1. The pin of port C is selected using bit select bits [b b b] and set or reset is decided by bit S/\bar{R} .
2. The BSR mode affects only one bit of port C at a time. The bit set using BSR mode remains set unless and until you change the bit. So to set any bit of port C, bit pattern is loaded in control register.
3. If a BSR mode is selected it will not affect I/Omode.

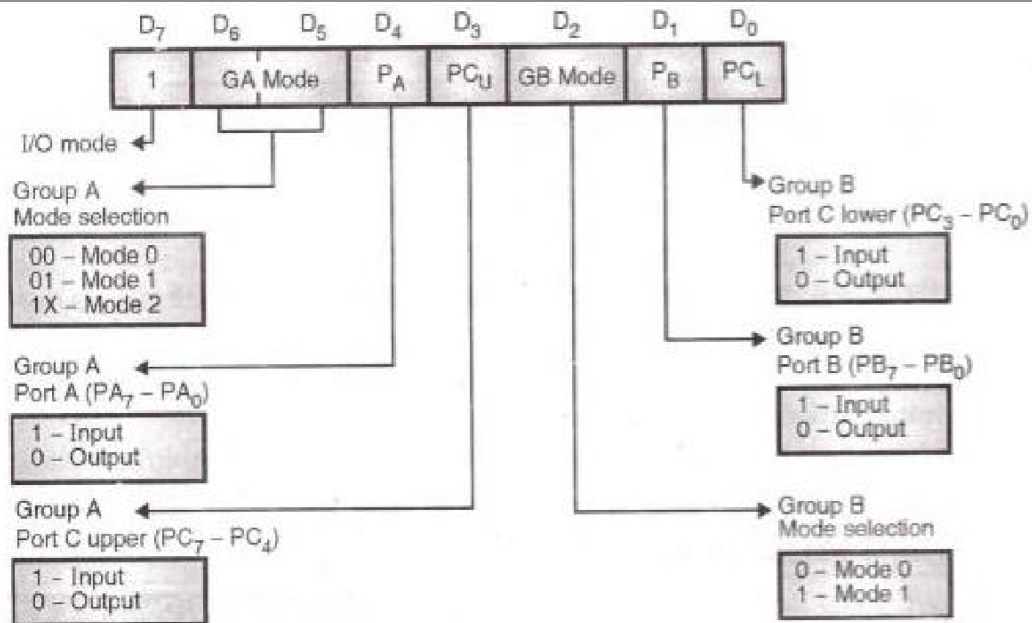
I/O modes

There are three I/O modes of operation:

- Mode 0- BasicI/O
- Mode 1- StrobedI/O
- Mode 2- Bi-directionalI/O

The I/O modes are programmed using control register.

The control word format of I/O modes is as shown in the figure below:



I/O modes control word format

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Function of each bit is as follows:

1. $D7$ – When the bit $D7 = 1$ then I/O mode is selected, if $D7=0$ then BSR mode is selected. The function of bits $D0$ to $D6$ is independent on mode (I/O mode or BSRmode).
2. $D6$ and $D5$ -In I/O mode the bits $D6$ and $D5$ specifies the different I/O modes for group A i.e. Mode 0, Mode 1 and Mode 2 for port A and port Cupper.
3. $D2$ – In I/O mode the bit $D2$ specifies the different I/O modes for group B i.e. Mode 0 and Mode 1 forport B and port C lower.

All the 3 modes i.e. Mode 0, Mode 1 and Mode 2 are only for group A ports, but for group B only 2 modes i.e. Mode 0 and Mode 1 are provided. When 8255 is reset, it will clear control word register contents and all the ports are set to input mode. The ports of 8255 can be programmed for other modes by sending appropriate bit pattern to control register.

PA3	1	40	PA4	
PA2	2	39	PA5	
PA1	3	38	PA6	
PA0	4	37	PA7	
RD	5	36	WR	
CS	6	35	RESET	
gnd	7	34	D0	
A1	8	33	D1	
A0	9	32	D2	
PC7	10	8255	31	D3
PC6	11	PPI	30	D4
PC5	12	29	D5	
PC4	13	28	D6	
PC0	14	27	D7	
PC1	15	26	Vcc	
PC2	16	25	PB7	
PC3	17	24	PB6	
PB0	18	23	PB5	
PB1	19	22	PB4	
PB2	20	21	PB3	

Fig. 3.8 Pins of 8255

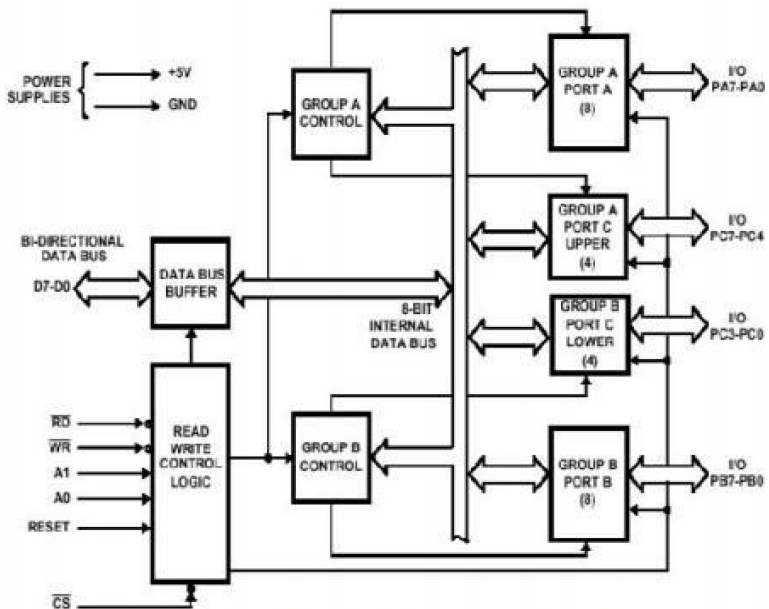


Fig.3.9 Block diagram of 8255

\overline{CS}	A ₁	A ₀	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	x	x	8255 is not selected

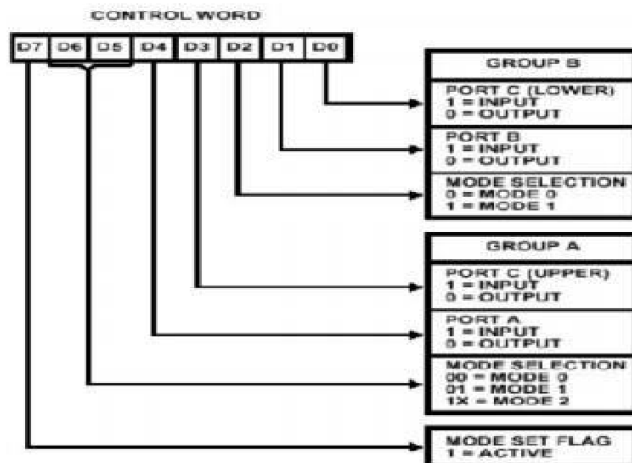


Fig 3.10 Control wordformat of8255

ü I/O Modes of 8255

Mode 0: Simple Input or Output

In this mode, Port A and Port B are used as two simple 8-bit I/O ports and Port C as two 4-bit I/O ports. Each port (or half-port, in case of Port C) can be programmed to function as simply an input port or an output port. The input/output features in mode 0 are: Outputs are latched, Inputs are not latched. Ports do not have handshake or interrupt capability.

Mode 1: Input or Output with handshake

In mode 1, handshake signals are exchanged between the microprocessor and peripherals prior to data transfer. The ports (A and B) function as 8-bit I/O ports. They can be configured either as input or output ports. Each port (Port A and Port B) uses 3 lines from port C as handshake signals. The remaining two

lines of port C can be used for simple I/O functions. Input and output data are latched and Interrupt logic is supported.

Mode 1: Input control signals

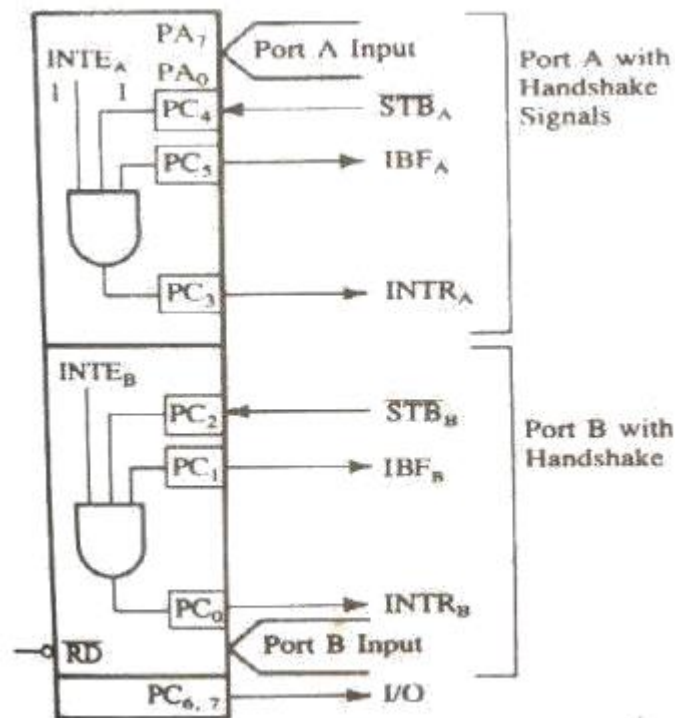


Fig.3.12 mode 1 input control signals

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

STB Strobe Input): This signal (active low) is generated by a peripheral device that it has transmitted a byte of data. The 8255, in response to, generates IBF and INTR.

IBF (Input buffer full): This signal is an acknowledgement by the 8255 to indicate that the input latch has received the data byte. This is reset when the microprocessor reads the data.

INTR (Interrupt Request): This is an output signal that may be used to interrupt the microprocessor. This signal is generated if , IBF and INTE are all at logic 1.

INTE (Interrupt Enable): This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTEA and INTEB are set /reset using the BSR mode. The INTEA is enabled or disabled through PC4, and INTEB is enabled or disabled throughPC2.

(Output Buffer Full): This is an output signal that goes low when the microprocessor writes data into the output latch of the 8255. This signal indicates to an output peripheral that new data is ready to be read. It goes high again after the 8255 receives a signal from the peripheral.

(Acknowledge): This is an input signal from a peripheral that must output a low when the peripheral receives the data from the 8255 ports.

INTR (Interrupt Request): This is an output signal, and it is set by the rising edge of the signal. This signal can be used to interrupt the microprocessor to request the next data byte for output. The INTR is set and INTE are all one and reset by the rising edge of . .

INTE (Interrupt Enable): This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTEA and INTEB are set /reset using the BSR mode. The INTEA signal can be enabled or disabled through PC6, and INTEB is enabled or disabled through PC2.

Mode 2: Bidirectional Data Transfer

OBF This mode is used primarily in applications such as data transfer between the two computers or floppy disk controller interface. Port A can be configured as the bidirectional port and Port B either in mode 0 or mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three lines from Port C can be used either as simple I/O or as handshake signals for Port B.

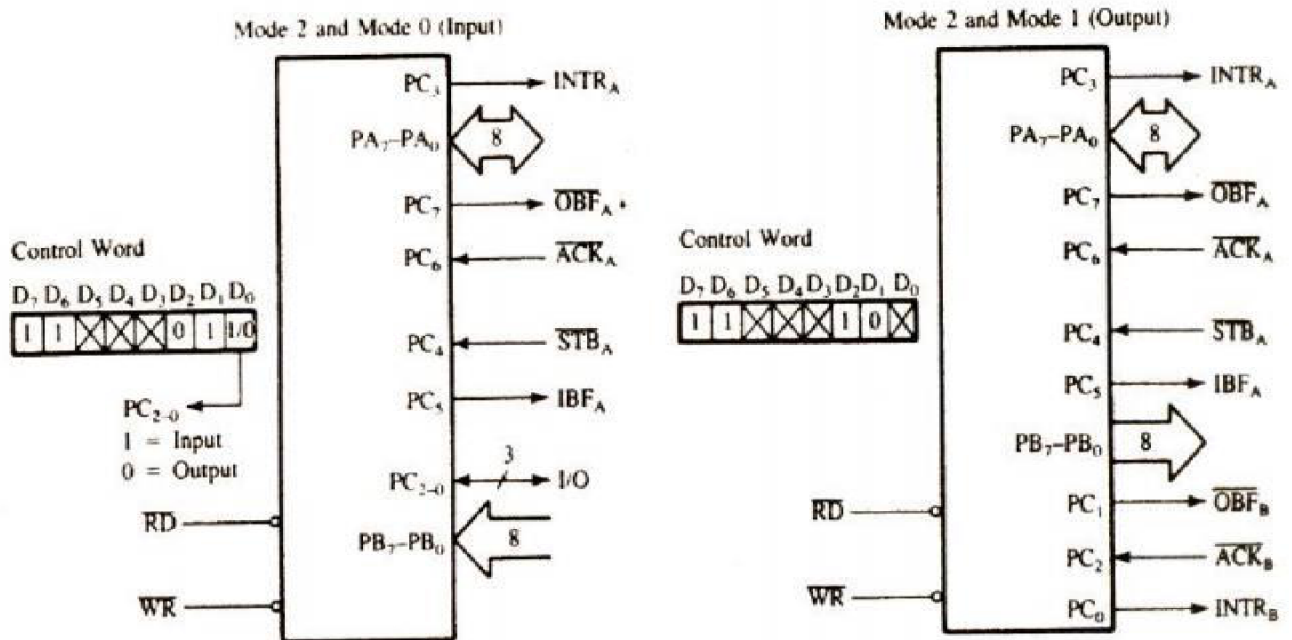


Fig. 3.14 Mode 2 Control Signals

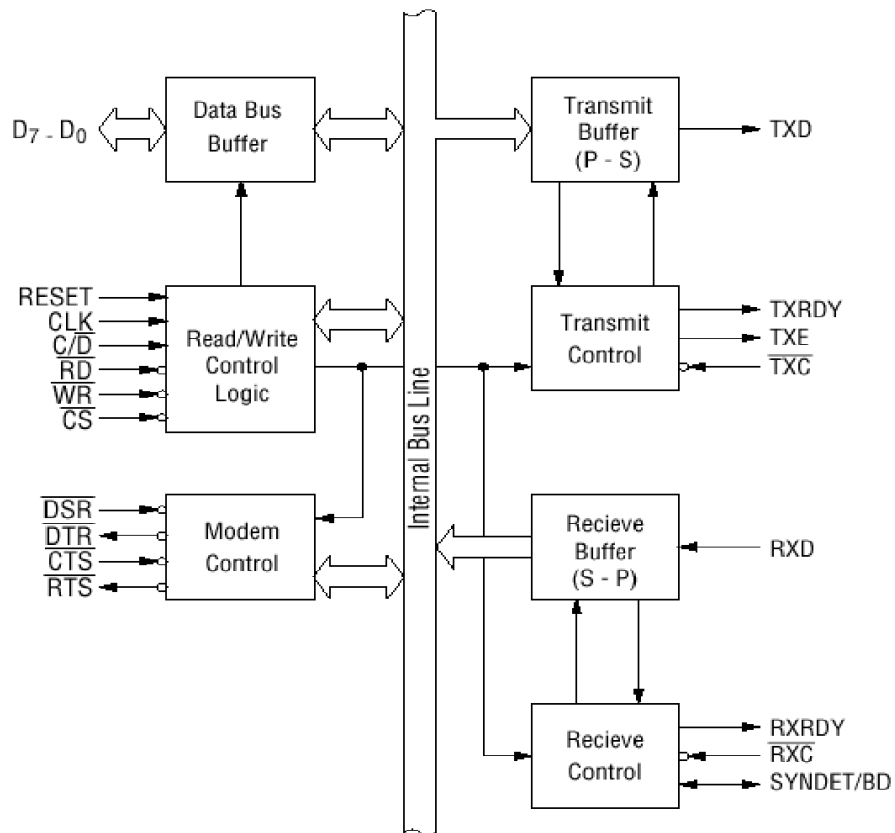
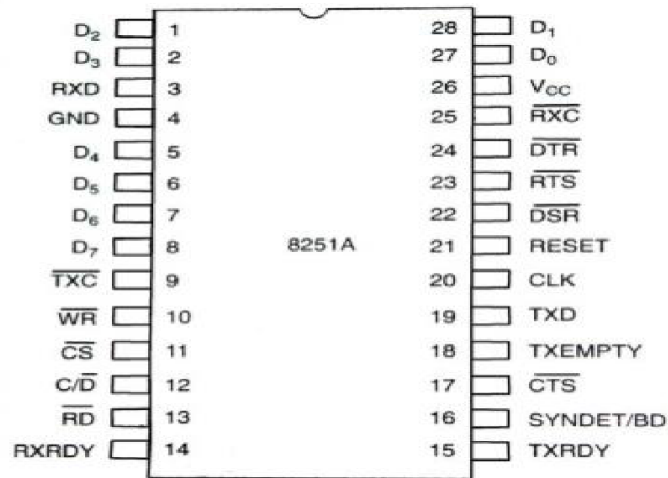
[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

SERIAL COMMUNICATION INTERFACE -PROGRAMMABLE COMMUNICATION INTERFACE(INTEL 8251)

The 8251 is a programmable chip designed for synchronous and asynchronous serial data communication. **USART (Universal Synchronous/Asynchronous Receiver/Transmitter)** is the key component for converting parallel data to serial form and vice versa Two types of serial data communications are widely used

- Asynchronous communications
- Synchronous communications

Pin diagram of 8251



Block diagram of 8251 [Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Signal Description of 8251

D 0 to D 7 (I/O terminal)

This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)

A "High" on this input forces the 8251 into "reset status." The device waits for the writing of "mode instruction." The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)

CLK signal is used to generate internal device timing. CLK signal is independent of RXC or TXC.

However, the frequency of CLK must be greater than 30 times the RXC and TXC at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

WR (Input terminal)

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the 8251.

RD (Input terminal)

This is the "active low" input terminal which receives a signal for reading receive data and status words from the 8251.

C/D (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the 8251 is accessed by the CPU. If C/D = low, data will be accessed. If C/D = high, command word or status word will be accessed.

CS (Input terminal)

This is the "active low" input terminal which selects the 8251 at low level when the CPU accesses. Note: The device won't be in "standby status"; only setting CS = High.

TXD (output terminal)

This is an output terminal for transmitting data from which serial-converted data is sent out. The device is in "mark status" (high level) after resetting or during a status when transmit is disabled. It is also possible to set the device in "break status" (low level) by a command.

TXRDY (output terminal)

This is an output terminal which indicates that the 8251 is ready to accept a transmitted data character. But the terminal is always at low level if CTS = high or the device was set in "TX disable status" by a command. Note: TXRDY status word indicates that transmit data character is receivable, regardless of CTS or command. If the CPU writes a data character, TXRDY will be reset by the leading edge of WR signal.

TXEMPTY (Output terminal)

This is an output terminal which indicates that the 8251 has transmitted all the characters and had no data character. In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted. If the CPU writes a data character, TXEMPTY will be reset by the leading edge of WR signal.

TXC (Input terminal)

This is a clock input signal which determines the transfer speed of transmitted data. In "synchronous mode," the baud rate will be the same as the frequency of TXC. In "asynchronous mode", it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16 or 1/64 the TXC. The falling edge of TXC sifts the serial data out of the 8251.

RXD (input terminal)

This is a terminal which receives serial data.

RXRDY (Output terminal)

This is a terminal which indicates that the 8251 contains a character that is ready to READ. If the CPU reads a data character, RXRDY will be reset by the leading edge of RD signal. Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

RXC (Input terminal)

This is a clock input signal which determines the transfer speed of received data. In "synchronous mode," the baud rate is the same as the frequency of RXC. In "asynchronous mode," it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16, 1/64 the RXC.

SYNDET/BD (Input or output terminal)

This is a terminal whose function changes according to mode. In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset. In "external synchronous mode, "this is an input terminal. A "High" on this input forces the 8251 to start receiving data characters.

In "asynchronous mode," this is an output terminal which generates "high level" output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level. After Reset is active, the terminal will be output at low level.

DSR (Input terminal)

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

DTR (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of DTR by a command.

CTS (Input terminal)

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmittable if the terminal is at low level.

RTS (Output terminal)

This is an output port for MODEM interface. It is possible to set the status RTS by a command.

The 8251 functional configuration is programmed by software. Operation between the 8251 and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

\overline{CS}	C/D	\overline{RD}	\overline{WR}	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	Status → CPU
0	1	1	0	Control Word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

Table 1 Operation between a CPU and 8251 [Source: **Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi**]

Control Words

There are two types of control word.

1. Mode instruction (setting of function)
2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the 8251. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."

Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- Number of synchronous characters (Synchronous mode)

The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of synchronous mode, it is necessary to write one or two byte sync characters. If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

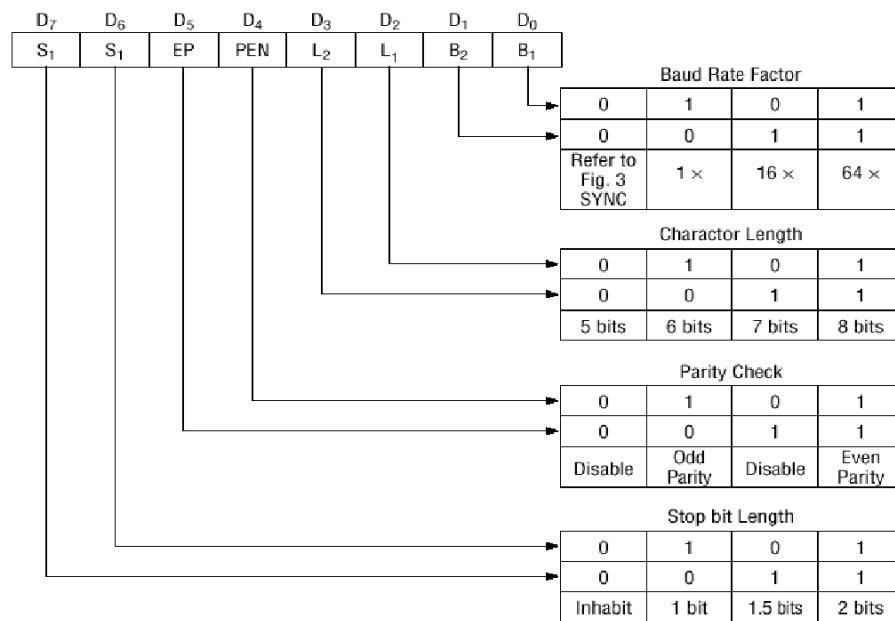


Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)

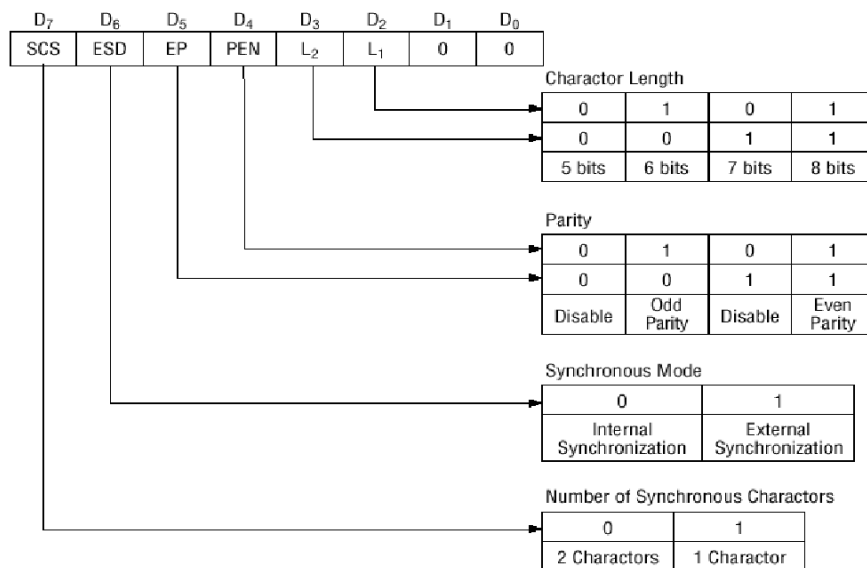


Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

2) Command

Command is used for setting the operation of the 8251. It is possible to write a command whenever necessary after writing a mode instruction and sync characters. Items to be set by command are as follows:

- Transmit Enable/Disable
- ReceiveEnable/Disable
- DTR, RTS Output of data.
- Resetting of errorflag.
- Sending to breakcharacters
- Internalresetting
- Hunt mode (synchronous mode)

Status Word

It is possible to see the internal status of the 8251 by reading a status word. The bit configuration of status word is shown in Fig. 5.

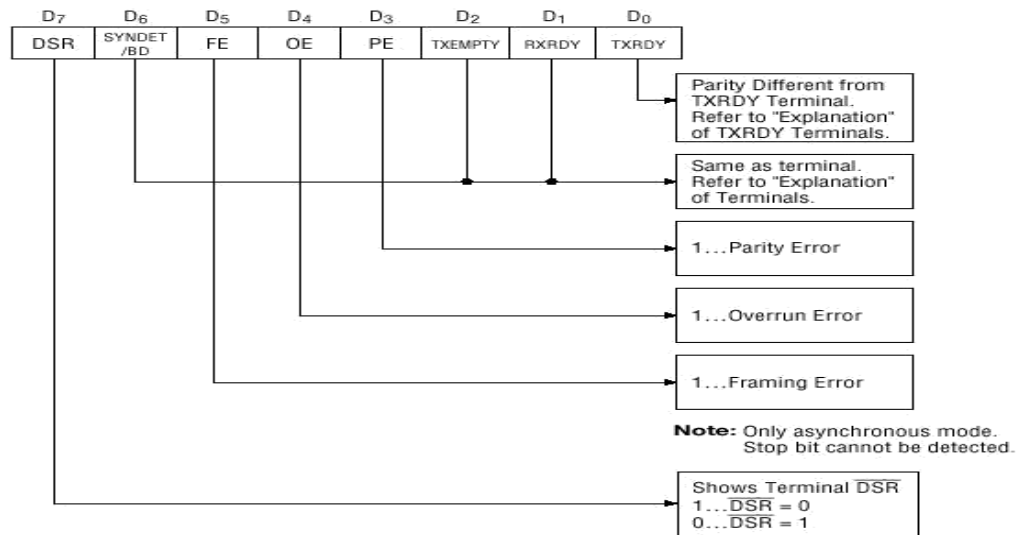


Fig. 5 Bit Configuration of Status Word

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

PROGRAMMABLE INTERVAL TIMER (8253/8254)

The Intel 8253 and 8254 are Programmable Interval Timers (PTIs) designed for microprocessors to perform timing and counting functions using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for "OUT" output. To operate a counter, a 16-bit count is loaded in its register. On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

Difference between 8253 and 8254

8253	8254
Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
It uses N-MOS technology	It uses H-MOS technology
Read-Back command is not available	Read-Back command is available
Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.

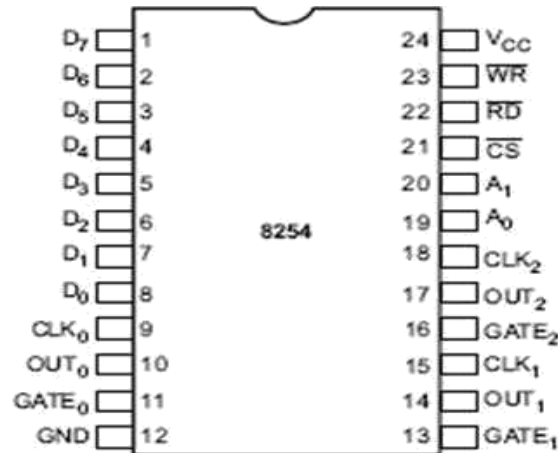
Features of 8253 / 54

The most prominent features of 8253/54 are as follows –

- It has three independent 16-bit down counters. These three counters can be programmed for either binary or BCD count.
- It can handle inputs from DC to 10MHz.
- It is compatible with almost all microprocessors.
- 8254 has a powerful command called READ BACK command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

8254 Architecture and Pin Description

PIN DETAILS OF 8254



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

CS - Chip select .When it is low, enables the communication between CPU and 8253.

WR-When it is low, the CPU output data in the form of mode information are loading counters.

RD – When it is low, the CPU reads data.

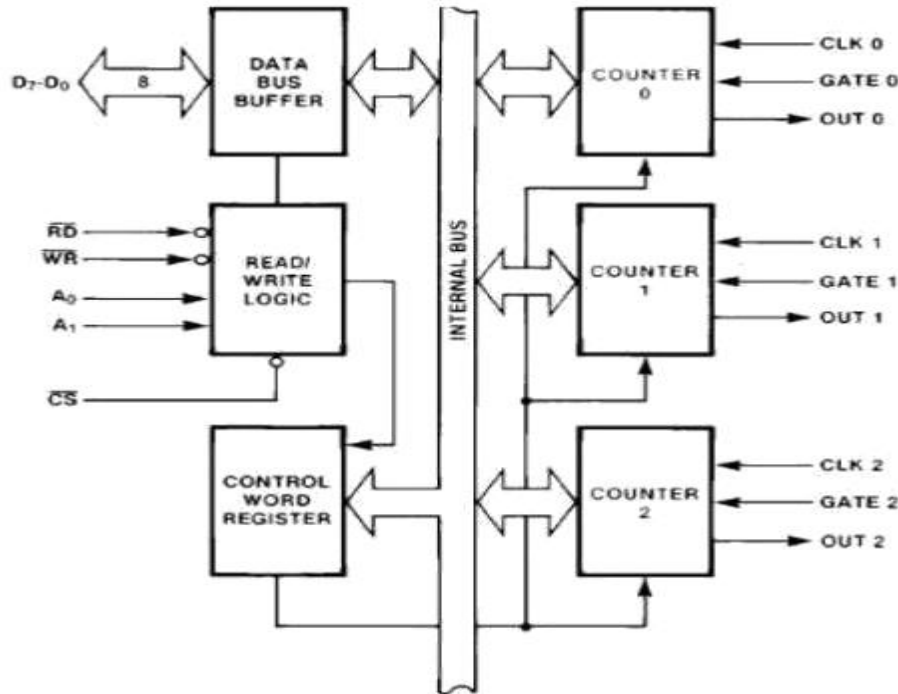
A0-A1: These pins are connected to address bus. These are used to select one of the three counters.

D0-D7: These are tri-state bidirectional data bus used to interface 8253 to the system data bus.

CLK0,CLK1,CLK2-These are clock signals for counter0, counter1 and counter2.

GATE0,GATE1,GATE2- These are gate terminals for counter0, counter1 and counter2.

OUT0,OUT1,OUT2- These are output terminals for counter0, counter1 and counter2.



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

In the above figure, there are three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals - CLOCK & GATE, and one output signal - OUT.

Data Bus Buffer

It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has three basic functions –

- Programming the modes of 8253/54.
- Loading the count registers.
- Reading the count values.

Read/Write Logic

It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW.

Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

A ₁	A ₀	Result
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register
X	X	No Selection

Control Word Register

This register is accessed when lines A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation.

Following table shows the result for various control inputs.

A ₁	A ₀	RD	WR	CS	Result
0	0	1	0	0	Write Counter 0
0	1	1	0	0	Write Counter 1
1	0	1	0	0	Write Counter 2
1	1	1	0	0	Write Control Word
0	0	0	1	0	Read Counter 0
0	1	0	1	0	Read Counter 1
1	0	0	1	0	Read Counter 2
1	1	0	1	0	No operation
X	X	1	1	0	No operation
X	X	X	X	1	No operation

Counters

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

Control Word Register:

Control Word Format

D7	D6	D5	D4	D3	D2	D1	D0
SC0	SC1	RL1	RL0	M2	M1	M0	BCD

When the pins A0,A1 are 11,the control word register is selected.

The bits D7 and D6 of the control word are to select one of the 3 counters.D5 and D4 are for loading /reading the count.D3,D2 and D1 are for the selection of operating mode of the selected counter.

SC-Select Counter The SC₀ and SC₁ bits of the control word select a counter.The selection of counters is given below:

SC ₁	SC ₀	Select Counter
0	0	Select Counter-0
0	1	Select Counter-1
1	0	Select Counter-2
1	1	Illegal

RL-Read/Load The RL_0 and RL_1 are used to load/read counts as follows:

RL_1	RL_0	Read /Load
0	0	Counter latching operation
0	1	Read/Load least significant byte only
1	0	Read/Load most significant byte only
1	1	Read/Load least significant byte first, then most significant byte

M-Mode Mode selecting bits M_0, M_1 and M_2 select any one of six modes given below:

M_2	M_1	M_0	Mode
0	0	0	Mode-0
0	0	1	Mode-1
X	1	0	Mode-2
X	1	1	Mode-3
1	0	0	Mode-4
1	0	1	Mode-5

BCD

- 0 Binary Counter, 16-bits
- 1 Binary Coded Decimal(BCD) counter (4 Decade)

Operation of 8253:

The complete functional definition of the 8253/54 is programmed by the system software. Once programmed, the 8253/54 is ready to perform whatever timing tasks it is assigned to accomplish.

WRITE Operation:

- Write a control word into control register.
- Load the low-order byte of a count in the counter register.
- Load the high-order byte of count in the counter register.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RW_1	RW_0	M_2	M_1	M_0	BCD

SC - Select counter

SC_1	SC_0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegal for 8253 Read -Back command for 8254 (See Read operations)

M - Mode

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW - Read /Write

RW_1	RW_0	
0	0	Counter latch command (See Read operations)
0	1	Read / Write least significant byte only
1	0	Read / Write most significant byte only
1	1	Read / write least significant byte first, then most significant byte

BCD :

0	Binary counter 16 - bits
1	Binary coded decimal (BCD) Counter (4 Decades)

Note : Don't care bits (x) should be 0 to ensure compatibility with future Intel products

1. Simple Read : It involves reading a count after inhibiting the counter by controlling the gate input or the clock input of the selected counter, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high orderbyte.

2. Counter Latch Command : In the second method, an appropriate control word is written into the control register to latch a count in the output latch, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high orderbyte.

3. Read-Back Command (Available only for 8254) : The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current status of the OUT pin and Null count flag of the selectedcounter(s).

Below figure shows the format of the control word register for Read-Back command.

$$A_0, A_1 = 11 \quad \overline{CS} = 0 \quad \overline{RD} = 1 \quad \overline{WR} = 0$$

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	COUNT	STATUS	CNT ₂	CNT ₁	CNT ₀	0

D₅ : 0 = Latch count of selected counter(s)

D₄ : 0 = Latch status of selected counter(s)

D₃ : 1 = Select counter 2

D₂ : 1 = Select counter 1

D₁ : 1 = Select counter 0

D₀ : Reserved for future expansion : must be 0.

8254 Modes of Operation:

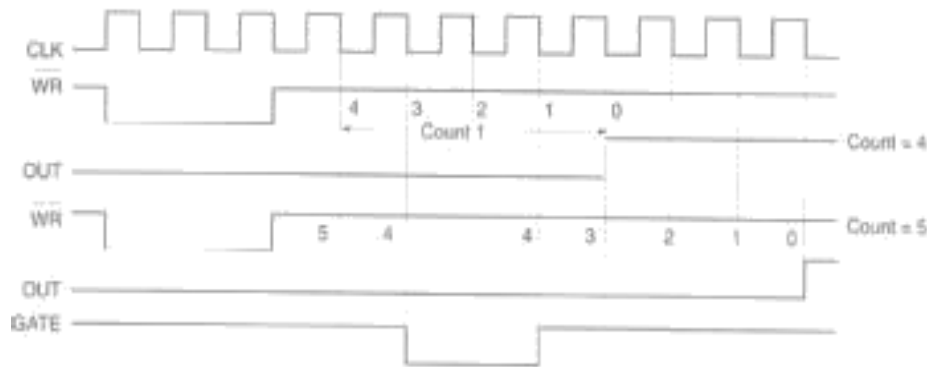
- 1.Mode 0 (Interrupt on terminal count)
- 2.Mode 1 (programmable Monoshot)
- 3.Mode 2 (Rate Generator)
- 4.Mode 3 (Square Wave Generator)
- 5.Mode 4 (Software Triggered Strobe)
- 6.Mode 5 (Hardware TriggeredStrobe)

Mode 0 (Interrupt on terminal count)

It is used to generate an interrupt to the microprocessor after pt to the microprocessor after a certain interval of a certain interval of time. The output is initially low after the mode is set. The output remains LOW after the count value is loaded in the counter.

The process of decrementing the counter continues till the terminal count is reached i.e., the count becomes zero and output goes HIGH.The output remains high until it reloads a new mode of operation or newcount.

The GATE signal is high for normal counting .When GATE goes low counting is terminated and the current count is latched till the GATE goes high again.

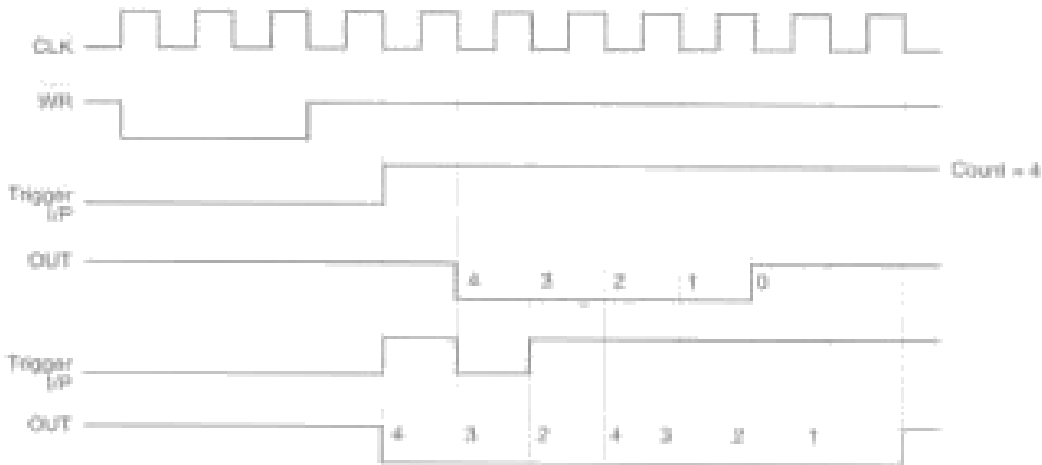


[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Mode 1: Programmable Monoshot

The 8253/8254 can be used as a monostable multivibrator.

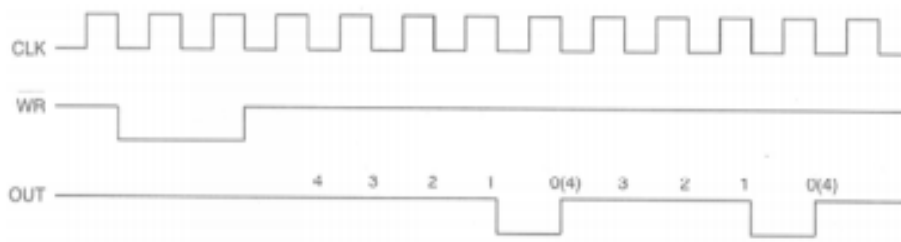
The gate input is used as trigger input in this mode. Normally, the output remains high until the count is loaded and a trigger is applied.



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Mode 2: Rate Generator

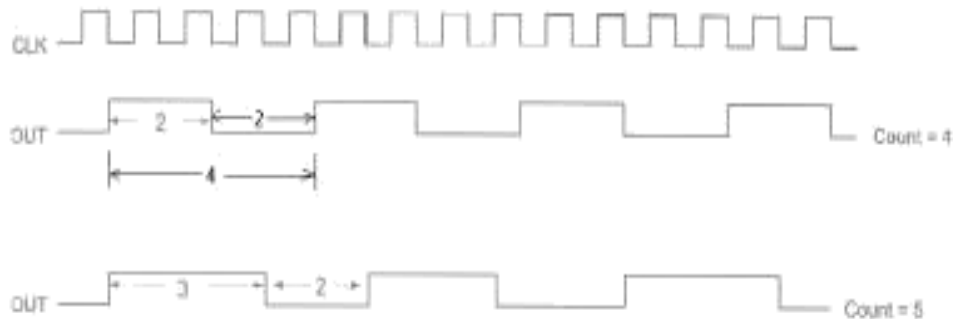
- Divide by N Counter
- The output is normally high after initialization
- If N is loaded as the count value, after N pulses, the output becomes low for one clock cycles.
- Whenever the count becomes zero another low pulse is generated at the output.



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Mode 3: Square wave rategenerator

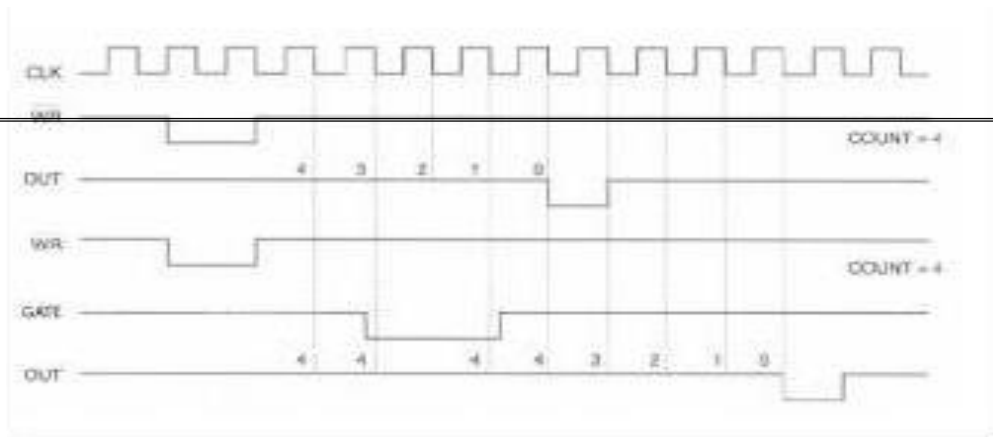
- It is similar to mode2
- When the count N is loaded is EVEN, half of the count will be high and half of the count will below.
- When, the count N is loaded is ODD, the $N+1/2$ count will be high and $N-1/2$ will be low.



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Mode 4: Software Triggered Strobe

- After the mode is set, the output goes high.
- The counter automatically begins to decrement (count down) one clock pulse after it is loaded with the initial value is loaded.
- When the GATE signal goes low the count is latched
- Once the terminal count, the output goes low for one clock cycle and then again goes high. this low pulse can be used as a strobe.



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

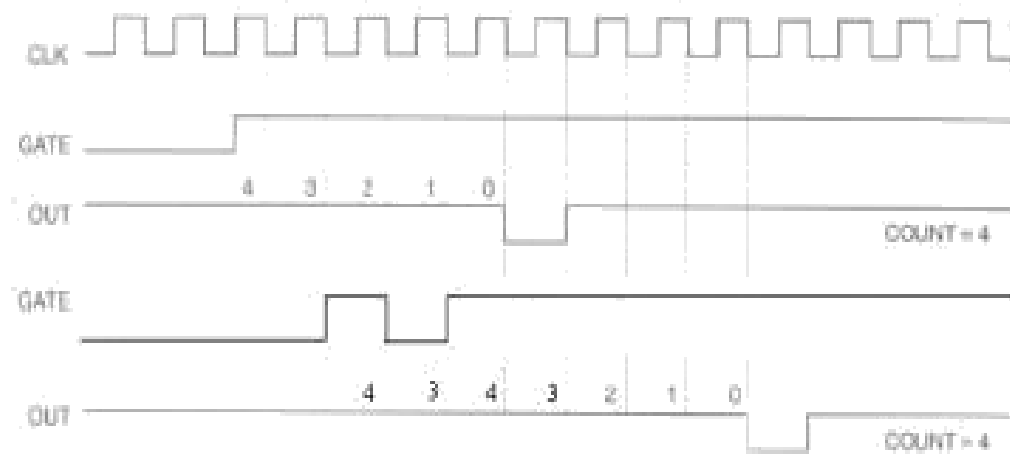
Mode 5: Hardware Triggered Strobe

This mode generates a strobe in response to an externally generated signal. It is similar to mode 4 except that the counting is initiated by a signal at the gate input.

After it is initialized, the output goes high.

The counter starts counting after the rising edge of the trigger input (GATE)

When the terminal count is reached, the output goes low for one clock cycle.



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

KEYBOARD /DISPLAY CONTROLLER 8279 - PROGRAMMABLE KEYBOARD CONTROLLER

8279 programmable keyboard/display controller is designed by Intel that interfaces a keyboard with the CPU. The keyboard first scans the keyboard and identifies if any key has been pressed. It then sends their relative response of the pressed key to the CPU and vice-a-versa.

How Many Ways the Keyboard is Interfaced with the CPU?

The Keyboard can be interfaced either in the interrupt or the polled mode.

In the **Interrupt mode**, the processor is requested service only if any key is pressed, otherwise the CPU will continue with its main task.

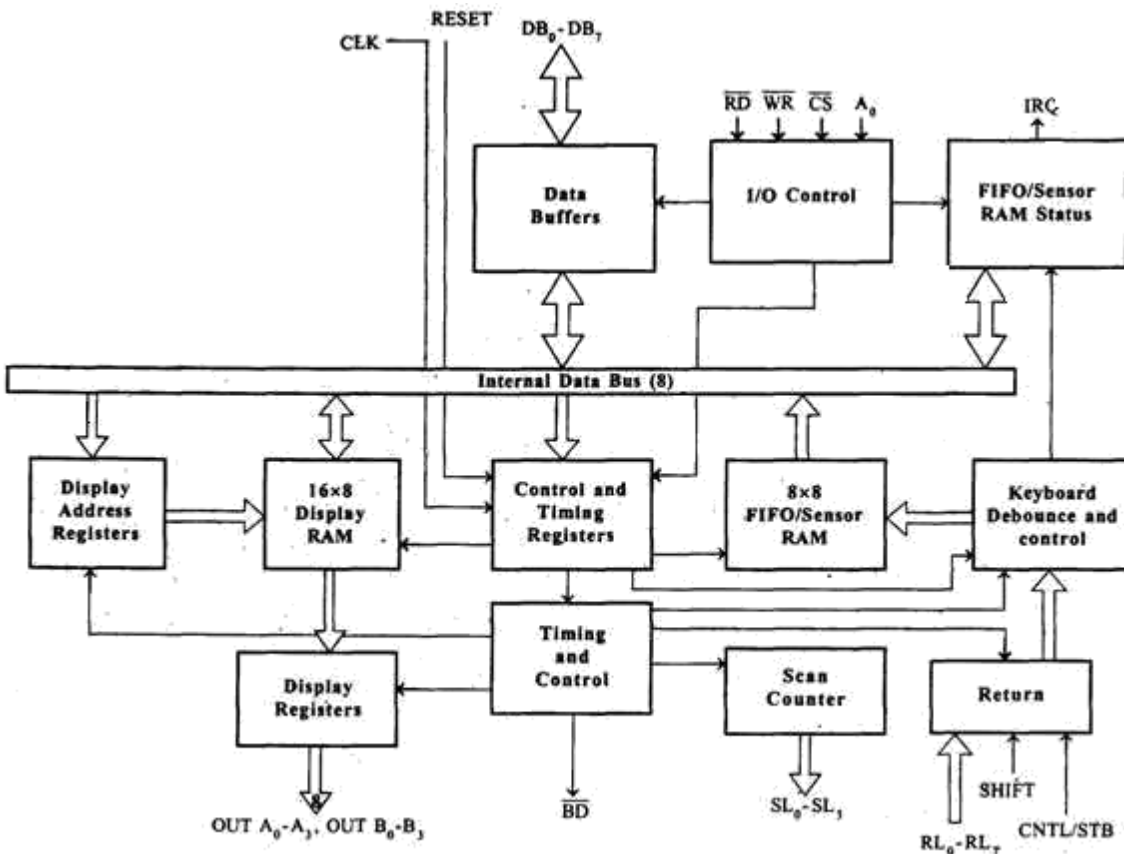
In the **Polled mode**, the CPU periodically reads an internal flag of 8279 to check whether any key is pressed or not with key pressure.

How Does 8279 Keyboard Work?

The keyboard consists of maximum 64 keys, which are interfaced with the CPU by using the key-codes. These key-codes are de-bounced and stored in an 8-byte FIFO RAM, which can be accessed by the CPU. If more than 8 characters are entered in the FIFO, then it means more than eight keys are pressed at a time. This is when the overrun status is set.

If a FIFO contains a valid key entry, then the CPU is interrupted in an interrupt mode else the CPU checks the status in polling to read the entry. Once the CPU reads a key entry, then FIFO is updated, and the key entry is pushed out of the FIFO to generate space for new entries.

Architecture and Description



Bhurchandi]

I/O Control and Data Buffer

This unit controls the flow of data through the microprocessor. It is enabled only when D is low. Its data buffer interfaces the external bus of the system with the internal bus of the microprocessor. The pins A0, RD, and WR are used for command, status or data read/write operations.

Control and Timing Register and Timing Control

This unit contains registers to store the keyboard, display modes, and other operations as programmed by the CPU. The timing and control unit handles the timings for the operation of the circuit.

Scan Counter

It has two modes i.e. **Encoded mode** and Decoded mode. In the encoded mode, the counter provides the binary count that is to be externally decoded to provide the scan lines for the keyboard and display.

In the **decoded scan mode**, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL₀-SL₃.

Return Buffers, Keyboard Debounce, and Control

This unit first scans the key closure row-wise, if found then the keyboard debounce unit debounces the key entry. In case, the same key is detected, then the code of that key is directly transferred to the sensor RAM along with SHIFT & CONTROL key status.

FIFO/Sensor RAM and Status Logic

This unit acts as 8-byte first-in-first-out (FIFO) RAM where the key code of every pressed key is entered into the RAM as per their sequence. The status logic generates an interrupt request after each FIFO read operation till the FIFO gets empty.

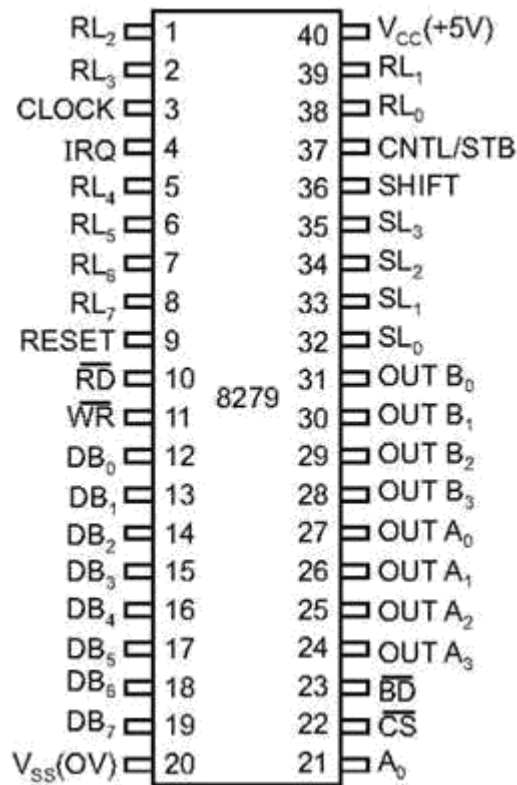
In the scanned sensor matrix mode, this unit acts as sensor RAM where its each row is loaded with the status of their corresponding row of sensors into the matrix. When the sensor changes its state, the IRQ line changes to high and interrupts the CPU.

Display Address Registers and Display RAM

This unit consists of display address registers which holds the addresses of the word currently read/written by the CPU to/from the display RAM.

8279 – Pin Description

The following figure shows the pin diagram of 8279 –



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Data Bus Lines, DB₀ - DB₇

These are 8 bidirectional data bus lines used to transfer the data to/from the CPU.

CLK

The clock input is used to generate internal timings required by the microprocessor.

RESET

As the name suggests this pin is used to reset the microprocessor.

CS Chip Select

When this pin is set to low, it allows read/write operations, else this pin should be set to high.

A₀

This pin indicates the transfer of command/status information. When it is low, it indicates the transfer of data.

RD, WR

This Read/Write pin enables the data buffer to send/receive data over the data bus.

IRQ

This interrupt output line goes high when there is data in the FIFO sensor RAM. The interrupt line goes low with each FIFO RAM read operation. However, if the FIFO RAM further contains any key-code entry to be read by the CPU, this pin again goes high to generate an interrupt to the CPU.

V_{ss}, V_{cc}

These are the ground and power supply lines of the microprocessor.

SL₀ – SL₃

These are the scan lines used to scan the keyboard matrix and display the digits. These lines can be programmed as encoded or decoded, using the mode control register.

RL₀ – RL₇

These are the Return Lines which are connected to one terminal of keys, while the other terminal of the keys is connected to the decoded scan lines. These lines are set to 0 when any key is pressed.

SHIFT

The Shift input line status is stored along with every key code in FIFO in the scanned keyboard mode. Till it is pulled low with a key closure, it is pulled up internally to keep it high.

CNTL/STB - CONTROL/STROBED I/P Mode

In the keyboard mode, this line is used as a control input and stored in FIFO on a key closure. The line is a strobe line that enters the data into FIFO RAM, in the strobed input mode. It has an internal pull up. The line is pulled down with a key closure.

BD

It stands for blank display. It is used to blank the display during digit switching.

OUTA₀ – OUTA₃ and OUTB₀ – OUTB₃

These are the output ports for two 16x4 or one 16x8 internal display refresh registers. The data from these lines is synchronized with the scan lines to scan the display and the keyboard.

Operational Modes of 8279

There are two modes of operation on 8279 – **Input Mode** and **Output Mode**.

Input Mode

This mode deals with the input given by the keyboard and this mode is further classified into 3 modes.

- **Scanned Keyboard Mode** – In this mode, the key matrix can be interfaced using either encoded or decoded scans. In the encoded scan, an 8x8 keyboard or in the decoded scan, a 4x8 keyboard can be interfaced. The code of key pressed with SHIFT and CONTROL status is stored into the FIFO RAM.

Scanned Keyboard Mode with 2 KeyLockout

In this mode of operation, when a key is pressed, debounce logic comes into operation. The Key code of the identified key is entered into the FIFO with SHIFT and CNTL status, provided the FIFO is not full.

Scanned Keyboard with N-keyRollover

In this mode, each key depression is treated independently. When a key is pressed, the debounce

circuit waits for 2 keyboard scans and then checks whether the key is still depressed. If it is still depressed, the code is entered in FIFO RAM. Any number of keys can be pressed simultaneously and recognized in the order, the Keyboard scan record them.

1. Scanned Keyboard Special ErrorMode

This mode is valid only under the N-Key rollover mode. This mode is programmed using end interrupt/error mode set command. If during a single debounce period (two Keyboard scan) two keys are found pressed, this is considered a simultaneous depression and an error flag is set. This flag, if set, prevents further writing in FIFO but allows generation of further interrupts to the CPU for FIFO read.

- **Scanned Sensor Matrix** – In this mode, a sensor array can be interfaced with the processor using either encoder or decoder scans. In the encoder scan, 8×8 sensor matrix or with decoder scan 4×8 sensor matrix can be interfaced.

- **Strobed Input** – In this mode, which is controlled by \overline{CS} set to 0, the data on the return lines is stored in the FIFO byte by byte.

Output Mode

This mode deals with display-related operations. This mode is further classified into two output modes.

- **Display Scan** – This mode allows 8/16 character multiplexed displays to be organized as dual 4-bit/single 8-bit display units.

- **Display Entry** – This mode allows the data to be entered for display either from the
 - Right entry (Calculator Type)
 - Left entry

Command Words of 8279

All the command words or status words are written or read with \overline{CS} = 1 and \overline{CS} = 0 to or from 8279. This section describes the various command words available for 8279.

- Keyboard Display Mode Set – The format of the command word to select different modes of operation of 8279 is given below with its bit definitions.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	A ₀
0	1	1	AI	A	A	A	A	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	A ₀
1	0	0	AI	A	A	A	A	1

Read Display RAM :

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

This command enables a programmer to read the display RAM data. The CPU writes this command word to 8279 to prepare it for display RAM read operation. AI is auto increment flag and AAAA, the 4-bit address points to the 16-byte display RAM that is to be read. If AI=1, the address will be automatically, incremented after each read or write to the Display RAM. The same address counter is used for reading and writing.

Write Display RAM :

AI – Auto increment Flag.

AAAA – 4 bit address for 16-bit display RAM to be written.

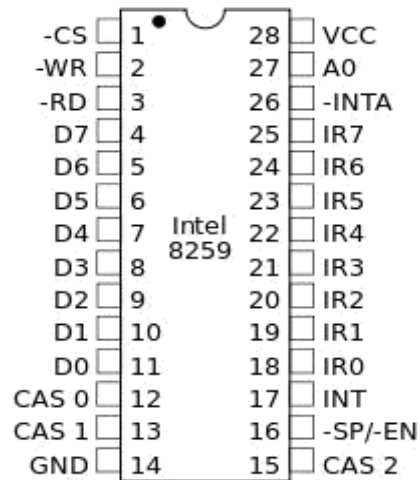
Programmable Interrupt Controller- INTEL 8259A

The 8259A is a programmable interrupt controller specially designed to work with Intel microprocessor 8080, 8085A, 8086, 8088. The main features of 8259A programmable interrupt controller are given below:

- 1) It can handle eight interrupt inputs. This is equivalent to providing eight interrupt pins on the processor in place of one INTR (in 8085A)/INT (in 8086) pin.
- 2) It can resolve eight levels of interrupt priorities in a variety of modes. The priorities of interrupts can be changed under running condition.
- 3) Each of the interrupt requests can be masked individually similar to RST7.5, RST6.5 and RST5.5 interrupts of 8085A.
- 4) The status of pending interrupts, in service interrupts, and masked interrupts can be read at any time similar to RST interrupts of 8085A.
- 6) The chip can be programmed to accept interrupt requests either as level triggered or edge triggered interrupt request unlike your RST interrupts where some are edge triggered and

some are level triggered. However, all interrupts must be either level triggered or edge triggered.

Pin Configuration of Intel 8259A



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

The 8259 A is contained in a 28 dual-in-line package that requires only +5V supply voltage. The 8259A is upward compatible with 8259. The main difference between the two is that the 8259A can be used with Intel 8086/8088 processor. It also includes additional features such as level triggered mode, buffered mode and automatic end of interrupt mode.

The pin diagram and internal block diagram of PIC is shown in figure. The pins are defined as follows:

CS (Chip Select signal): To access this chip, chip select signal CS is made low. A LOW on this pin enables RD & WR communication between the CPU and the 8259A. This signal is made LOW by decoding the addresses assigned to this chip. Therefore, this pin is connected to address bus through the decoder logic circuit. Interrupt acknowledge functions to transfer the control to interrupt service subroutine are independent of CS.

WR (Write signal): A low on this pin. When CS is low enables the 8259 A to accept command words from CPU.

RD (Read signal): A low on this pin when CS is low enables this 8259A to release status (pending interrupts or in-service interrupts or masked interrupts) on to the data bus for the CPU. The status includes the contents of IMR (interrupt mask register) or ISR (interrupt service register) or IRR (interrupt request register) or a priority level.

D₇-D₀ (Data Bus): Bidirectional data bus. Control, status and interrupt vector information is transferred via this data bus. This bus is connected to BDB of 8085A.

CAS₂-CAS₀ (Cascade lines): The CAS₂₋₀ lines form a local 8259A bus to control multiple 8259As in master-slave configuration, i.e., to identify a particular slave 8259A to be accessed for transfer of vector information. These pins are automatically set as output pins for master 8259A and input pins for a slave 8259A once the chips are programmed as master or slave.

SP/ EN (Slave Program/Enable Buffer): This is a dual function pin. When the chip is programmed in buffered mode, the pin can be used as an output and when not in the buffered mode it is used as an input. In non-buffered mode it is used as an input pin to determine whether the 8259A is to be used as a master (SP/ EN = 1) or as a slave (SP/ EN = 0).

INT (Interrupt output): This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin (INTR). In case of master-slave

configuration, the interrupt pin of slave 8259A is connected to interrupt request input of master 8259A.

INTA (Interrupt Acknowledge): This pin is used to enable 8259A interrupt vector data on the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

IR₀-IR₇ (Interrupt Request inputs): These are asynchronous interrupt request input pins. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged. (Edge triggered mode) or just by a high level on an interrupt request input (Level triggered mode).

A₀ (A₀ address line): This pin acts in conjunction with the RD , WR & CS pins. It is used by the 8259A to send various command words from the CPU and to read the status. It is normally connected to the CPU A₀ address line. Two addresses are assigned/ reserved in the I/O address space for each 8259A in the system- one with A₀=0 is called even address and other with A₀ = 1 is called odd address.

FunctionalDescription:

The 8259A (PIC) has eight interrupt request inputs – IR₇ - IR₀. The 8259A uses its INT output to interrupt the 8085A via INTR pin. The 8259A receives interrupt acknowledge pulses from the 8085A at its INTA input. Vector address, used by the 8085A to transfer control to the service subroutine of the interrupting device, is provided by the 8259A on the data bus. The 8259A is a programmable device that must be initialized by command words sent by the microprocessor. After initialization the 8259A mode of operation can be changed by operation command words from the microprocessor.

It contains following blocks-

1. Data busbuffer-

- It is used to transfer data between microprocessor and internal bus.

1. Read/write logic-

- It sets the direction of data bus buffer.
- It controls all internal read/write operations.
- It contains initialization and operation command registers.

Cascaded buffer and comparator-

- In master mode, it functions as a cascaded buffer. The cascaded buffers output slave identification number on cascade lines.
- In slave mode, it functions as a comparator. The comparator reads slave identification number from cascade lines and compares this number with its internal identification number.
- In buffered mode, it generates an (EN) signal.

Control logic-

- It generates an INT signal. In response to an (INTA) signal, it releases three byte CALL address or one byte vector number.
- It controls read/write control logic, cascade buffer/comparator, in service register, priority resolver and IRR.

Interrupt request register-

- It is used to store all pending interrupt requests.
- Each bit of this register is set at the rising edge or at the high level of the corresponding interrupt request line.
- The microprocessor can read contents of this register by issuing appropriate command word.

In service register (InSR)-

- It is used to store all interrupt levels currently being serviced.
- Each bit of this register is set by priority resolver and reset by end of interrupt command word.

- The microprocessor can read contents of this register by issuing appropriate commandword.

Priority resolver-

- It determines the priorities of the bit set in the IRR. To make decision, the priorityresolver looks at theISR.
- If the higher priority bit in the InSR is set then it ignores the newrequest.
- If the priority resolvers find that the new interrupt has a higher priority than the highest priority interrupt currently being serviced and the new interrupt is not in service, then it will set appropriate bit in the InSR and send the INT signal to the microprocessor for new interrupt request.

Interrupt mask register (IMR)-

- It is a programmable register.
- It is used to mask unwanted interrupt request by writing appropriate commandword.
- The microprocessor can read contents of this register without issuing any commandword.

Priority modes of 8259

1. Fully NestedModes

Defaultmode.

IR0 has the highest priority and IR7 has the lowest one.

If the ISR (in service) bit is set, all the same or lower priority interrupts are inhibited.

2. End OfInterrupt

The ISR bit can be reset either with AEOI bit of ICW1 or by EOI command.

Two types of EOI command;

- a) Specific
- b) Non-specific

The non-specific EOI command automatically reset the highest ISR bit.

When a mode that may disturb the fully nested structure, the specific EOI command is issued to reset a particular ISR bit.

An ISR bit that is masked by the corresponding IMR bit, will not be cleared by a non-specific EOI , if it is in special mode.

3. AutomaticRotation

Used in the applications where , all the interrupting devices are of equal priority.

In this mode, an IR level receives lowest priority after it is served while the next device to be served gets the highest priority in sequence.

4. Automatic EOIMode

Till AEOI=1 in ICW4, 8259A operates in AEOI mode.

The 8259A performs a non- specific EOI at the trailing edge of the last /INTA pulse automatically.

AEOI should be used only when a nested multilevel interrupt structure is not required.

5. SpecificRotation

A bottom priority level can be selected, using L2, L1 and L0 inOCW2 and R=1, SL=1,EOI=0. The selected bottom priority fixes other priorities.

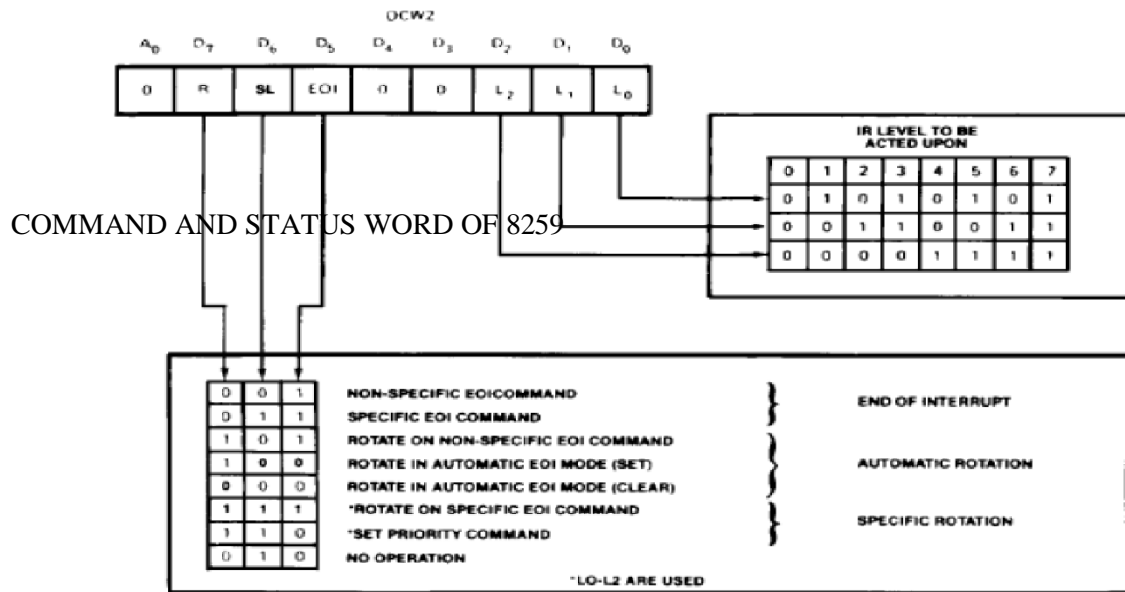


Fig1.7.b

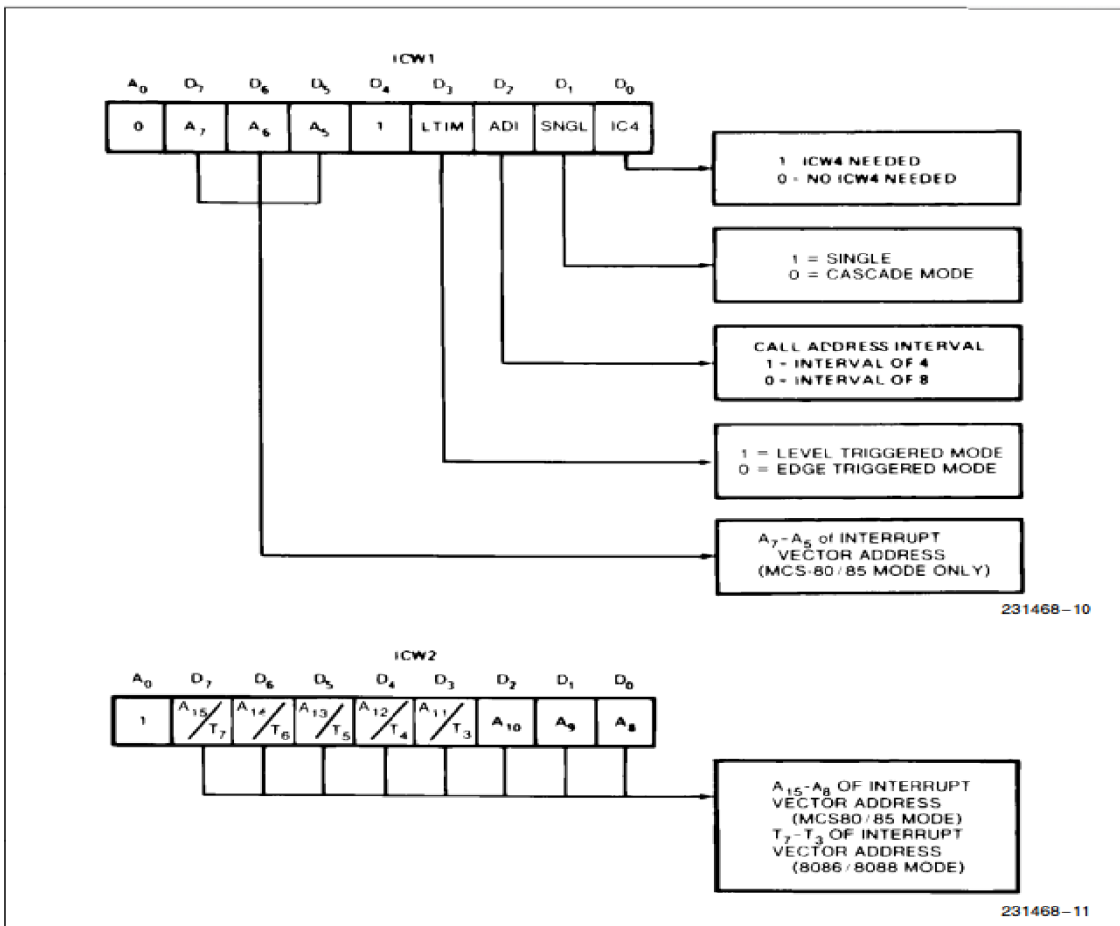


Figure 7. Initialization Command Word Format

DMA CONTROLLER(8257):DIRECT MEMORY ACCESS

It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

How DMA Operations are Performed?

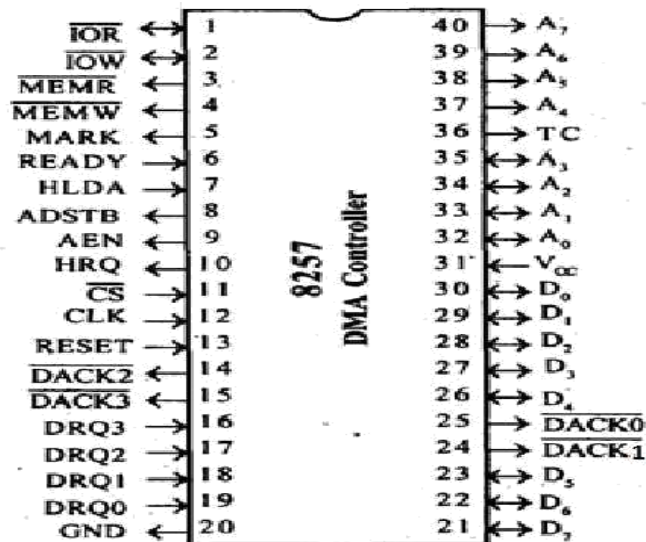
The sequence of operations performed by a DMA –

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Features of 8257

- It has four channels that can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode**.

8257 Pin Description



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

DRQ₀–DRQ₃

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ₀ has the highest priority and DRQ₃ has the lowest priority among them.

DACK₀ – DACK₃

These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

D₀ – D₇

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

A₀ - A₃

These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

A₄ - A₇

These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADST

This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

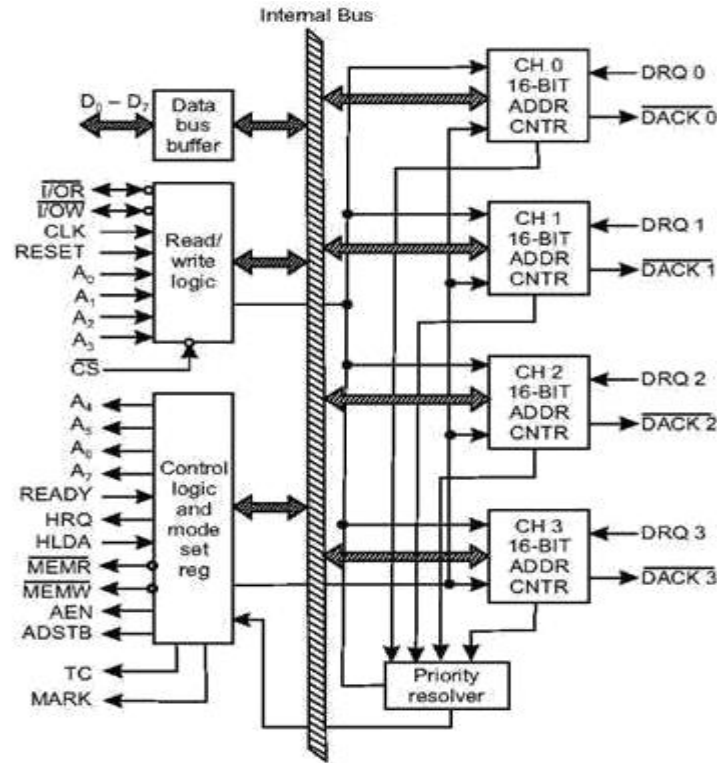
MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

V_{cc}

It is the power signal which is required for the operation of the circuit.

Internal Architecture of 8257:



[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

Data Bus Buffer:

The 8-bit, Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

Read/Write Logic:

In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the A₀-A₃ lines and either writes the contents of the data bus to the addressed internal register or reads the contents of the selected register depending upon whether IOW or IOR signal is activated.

In master mode, the read/write logic generates the IOR and IOW signals to control the data flow to or from the selected peripheral.

Control Unit:

The control logic controls the sequences of operations and generates the required control signals like AEN, ADSTB, MEMR, MEMW, TC and MARK along with the address lines A₄-A₇, in master mode.

Priority Resolver:

The priority resolver resolves the priority of the four DMA channels depending upon whether normal priority or rotating priority is programmed.

Register Organisation of 8257:

The 8257 performs DMA operation over four independent DMA channels such as

1. DMA Address Register

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting address stored in the DMA Address Register.

2. Terminal Count Registers

Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.

After each DMA cycle, the terminal count register content will be decremented by one and finally it becomes zero after the required number of DMA cycles are over.

The bits 14 and 15 of this register indicate the type of the DMA operation (transfer).

3. Mode Set Register

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation.

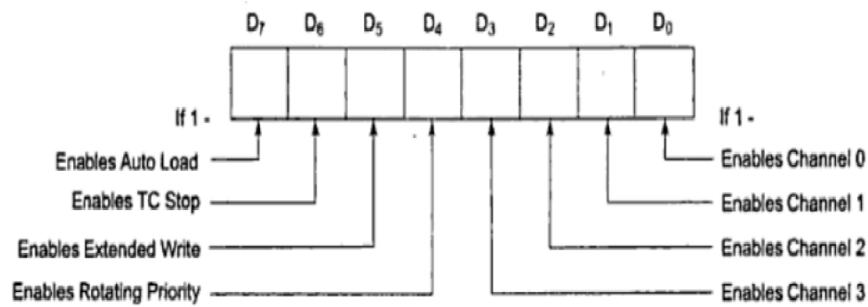


Fig. Bit Definitions of the Mode Set Register

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

The bits D₀-D₃ enable one of the four DMA channels of 8257

If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel.

If the TC STOP bit is programmed to be zero, the channel is not disabled, even after the count reaches zero and further request are allowed on the same channel.

The auto load bit, if set, enables channel 2 for the repeat block chaining operations, without immediate software intervention between the two successive blocks.

The extended write bit, if set to '1', extends the duration of MEMW and IOW signals by activating them earlier, this is useful in interfacing the peripherals with different access times.

4. Status register

The lower order 4-bits of this register contain the terminal count status for the four individual channels.

If any of these bits is set, it indicates that the specific channel has reached the terminal count condition.

The update flag is not affected by the read operation. This flag can only be cleared by resetting 8257.

The update flag is set every time, the channel 2 registers are loaded with contents of the channel 3 registers. It is cleared by the completion of the first DMA cycle of the new block. This register can only read.

DMA Transfer & Operations

The 8257 is able to accomplish three types of operations such

- as 1. DMA operation
- 2. Write Operation
- 3. Read Operation

The complete Operational sequence of 8257 is described in below state diagram.

- The 8257 request any one of the 8257 DRQ inputs to transfer single byte.
- In response to the request, the 8257 sends HRQ signal to CPU at its HLD input and waits for acknowledgement at the HLDA input.
- If the DMA controller receives the HLDA signal it indicates that the bus is available for the transfer.
- The DMA controllers generate the read and write commands to transfer the byte from/to the I/O Device.
- The DACK line of the used channel is pulled down by the dma controller to I/O device that its request for DMA transfers.
- The HRQ line is lowered by the DMA controller to indicate the CPU that it may regain the control of the bus.
- The DRQ must be high until acknowledged and must go low before S4 state of the DMA operation state diagram to avoid another unwanted transfer.
- In each s4 state ,the DRQ lines are sampled and highest priority request is recognized during next transfer. The HRQ line is maintained active till all the DRQ line go low.
- READY input used to interface 8257 with low speed devices. It is checked in s3 of the state diagram . S3=0 ,8257 enter wait state. S3=1 ,8257 continues from s4 to complete the transfer.

Interfacing DMA controller(8257) with 8086

If DMA controller is initialized by a CPU properly, it is ready to take control of the system bus on a DMA request, either from a peripheral or itself (in case of memory- to memory transfer). The DMA controller sends a HOLD request to the CPU and waits for the CPU to assert the HLDA signal. The CPU relinquishes the control of the bus before asserting the HLDA signal.

Once the HLDA signal goes high, the DMA controller activates the DACK signal to the requesting peripheral and gains the control of the system bus. The DMA controller is the sole master of the bus, till the DMA operation is over. The CPU remains in the HOLD status (all of its signals are tristate except HOLD and HLDA), till the DMA controller is the master of the bus.

The DMA controller interfacing circuit implements a switching arrangement for the address, data and control busses of the memory and peripheral subsystem from/to the CPU to/from the DMA controller.

