ELECTRONICS CIRCUITS I

SUBJECT CODE : EC 8351
YEAR / SEMESTER : II / III

SYLLABUS

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EC8351 ELECTRONIC CIRCUITS I

UNIT I BIASING OF DISCRETE BJT, JFET AND MOSFET 9

BJT– Need for biasing - DC Load Line and Bias Point – DC analysis of Transistor circuits - Various biasing methods of BJT – Bias Circuit Design - Thermal stability - Stability factors - Bias compensation techniques using Diode, thermistor and sensistor – Biasing BJT Switching Circuits- JFET - DC Load Line and Bias Point - Various biasing methods of JFET - JFET Bias Circuit Design - MOSFET Biasing - Biasing FET Switching Circuits.

UNIT II BJT AMPLIFIERS 9

Small Signal Hybrid π equivalent circuit of BJT – Early effect - Analysis of CE, CC and CB amplifiers using Hybrid π equivalent circuits - AC Load Line Analysis- Darlington Amplifier - Bootstrap technique - Cascade, Cascode configurations - Differential amplifier, Basic BJT differential pair – Small signal analysis and CMRR.

UNIT III SINGLE STAGE FET, MOSFET AMPLIFIERS 9

Small Signal Hybrid π equivalent circuit of FET and MOSFET - Analysis of CS, CD and CG amplifiers using Hybrid π equivalent circuits - Basic FET differential pair- BiCMOS circuits.

UNIT IV FREQUENCY RESPONSE OF AMPLIFIERS 9

Amplifier frequency response – Frequency response of transistor amplifiers with circuit capacitors – BJT frequency response – short circuit current gain - cut off frequency – $f\alpha$, $f\beta$ and unity gain bandwidth – Miller effect - frequency response of FET - High frequency analysis of CE and MOSFET CS amplifier - Transistor Switching Times.

UNIT V POWER SUPPLIES AND ELECTRONIC DEVICE TESTING 9

Linear mode power supply - Rectifiers - Filters - Half-Wave Rectifier Power Supply - Full-Wave Rectifier Power Supply - Voltage regulators: Voltage regulation - Linear series, shunt and switching Voltage Regulators - Over voltage protection - BJT and MOSFET – Switched mode power supply (SMPS) - Power Supply Performance and Testing - Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

TOTAL: 45 PERIODS

TEXT BOOK:(T)

1. T1.Donald. A. Neamen, Electronic Circuits Analysis and Design, 3rd Edition, Mc Graw HillEducation (India) Private Ltd., 2010. (Unit I-IV).
2. T2. Robert L.Boylestad and Louis Nasheresky, "Electronic Devices and Circuit Theory",11th Edition, Pearson Education,2013. (Unit V)

REFERENCES:(R)

1. R1.Millman J, Halkias.C.andSathyabradaJit, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2015.
2. R2.Salivahanan and N. Suresh Kumar, Electronic Devices and Circuits, 4th Edition, , Mc Graw Hill Education (India) Private Ltd., 2017.
3. R3.Floyd, Electronic Devices, Ninth Edition, Pearson Education, 2012.
4. R4.David A.Bell, Electronic Devices & Circuits, 5th Edition, Oxford University Press,2008.
5. R5.Anwar A. Khan and Kanchan K. Dey, A First Course on Electronics, PHI, 2006.
6. R6.Rashid M, Microelectronics Circuits, Thomson Learning, 2007

UNIT I

BIASING OF DISCRETE BJT, JFET AND MOSFET

BJT– Need for biasing - DC Load Line and Bias Point – DC analysis of Transistor circuits - Various biasing methods of BJT – Bias Circuit Design - Thermal stability - Stability factors - Bias compensation techniques using Diode, thermistor and sensistor – Biasing BJT Switching Circuits- JFET - DC Load Line and Bias Point - Various biasing methods of JFET - JFET Bias Circuit Design - MOSFET Biasing - Biasing FET Switching Circuits.

UNIT 1

BIASING OF DISCRETE BJT, JFET AND MOSFET

Bipolar Junction Transistor

- In 1904 to 1947 the vacuum tube was the electronic device. It was introduced by J. A Fleming as Vacuum tube diode later two years.
- In 1906 Lee De Forest added a third element called control grid to the vacuum tube and diode resulting the first amplifier, the triode.
- On December 23, 1947 Walter H Brattain and John Bardeen demonstrated the amplying action of the first transistor at Bell Laboratories.
- Transistor is a three terminal device. Base, emitter and collector can be operated as 3 configurations.

  Common Base
  Common Emitter
  Common Collector.

- A transistor can be used as an amplifier, switch, the concept of transfer of resistance has given the name TRANS for -resISTOR TRANSISTOR.
- According to the configuration it can be used for Voltage as well as current amplification.

There are two types of transistors.

* Unipolar junction Transistor
* Bipolar junction Transistor.

✓ In the unipolar junction transistors the current conduction is due to only one type of charge carriers ie, majority carriers.

✓ In case of bipolar junction transistor the current conduction is both the type of carriers. [holes & electrons]

✓ Thats why it is called bipolar junction transistor BJT. In BJT the output current is controlled by input current. Hence it is called current controlled device.

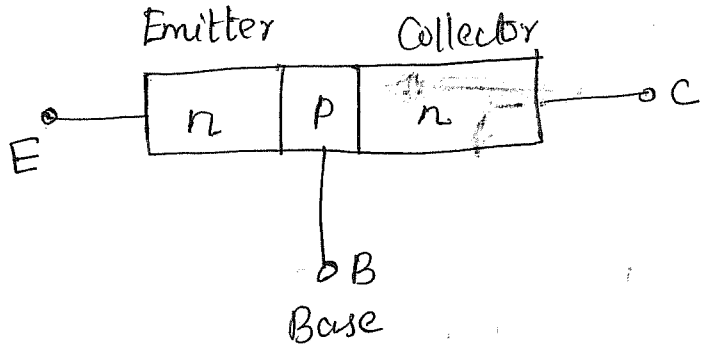
There are two types of BJT. They are

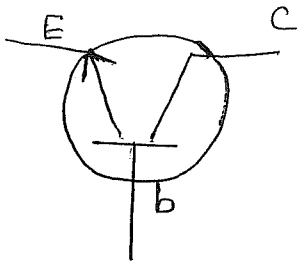
(i) n-p-n Type
(ii) p-n-p Type.

Structure of BJT

When a sigle 'p' region is sandwitched between two 'n' regions then it is called n-p-n transistor. When a single n region is sandwitched between two p type regions then that transistor is called pnp transistor.

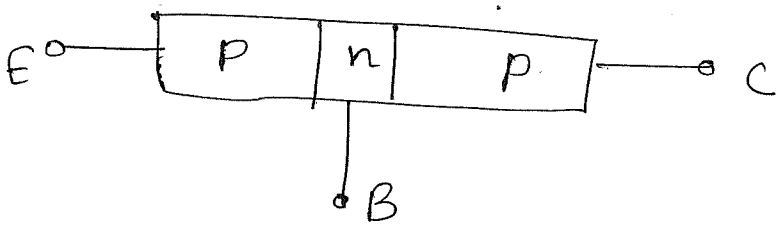
n-p-n

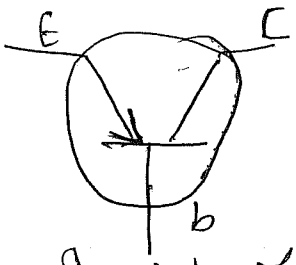




Symbol of n-p-n

p-n-p





Symbol of p-n-p.

The middle region of each transistor type is called base. Base is very thin and lightly doped.

Doping

The process by which impurities are added to a pure semiconductor is called doping. Base region is lightly doped. The other two regions emitter and collector regions. i'e) are heavily doped. ie, Emitter region is doping level is slightly greater than the collector region. The collector region area is slightly more than emitter area.

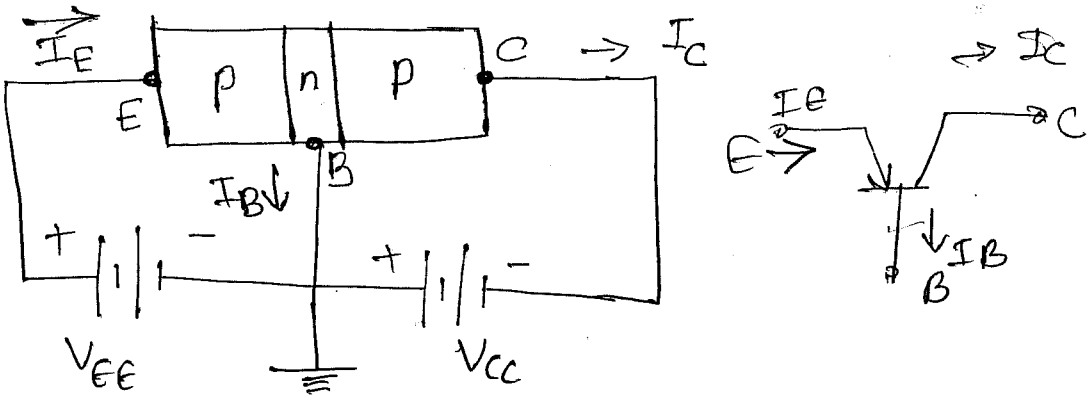
Transistor has two junctions. One junction is

(i) Emitter base junction (J_E)

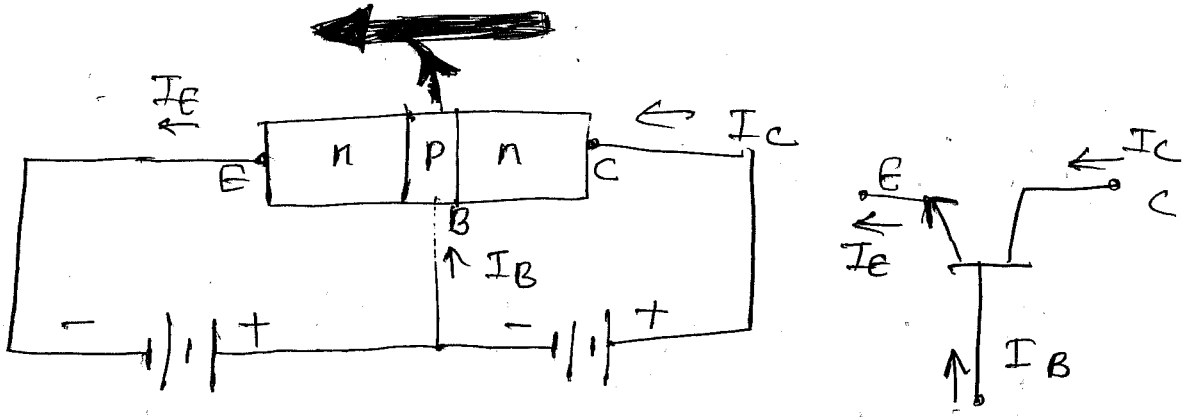
(ii) Collector Base junction (J_C)

Transistor Operation

Transistor Currents



npn



* The arrow at the emitter of the transistor's symbol points in the direction of conventional current. [ie the current flow from +ve to -ve]

Let us consider the pnp transistor. The current flowing into the emitter terminal is referred as the emitter current I_E. The current flows out of the collector and base terminals are Collector Current(I_C) and Base current I_B.

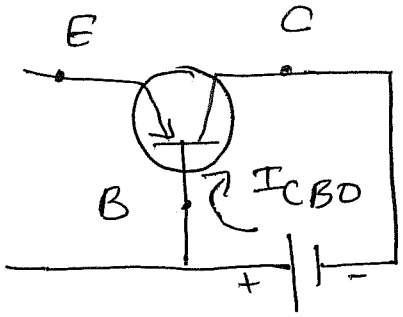
Reverse Collector Saturation Current (I_{CBO})

The I_{CBO} is nothing but the I_{CO} (Reverse Saturation Current) for a physical (real, non idealized transistor. It also defined as the current when emitter current is zero. As I_{CBO} is defined for physical transistor, it consistules the leakage current flowing around the junction and across the surfaces. Due to this $|I_{CBO}|$ exceeds $|I_{CO}|$. The other reason ~~I_{CO}~~ I_{CBO} exceeds I_{CO} is that new carriers may be generated by collision in the collector junction leading to avalanche multiplication of current.

I_{CBO}

Case:1 When emitter is open circuited

$I_C = I_{CBO}$



The emitter is open circuited. Since no carriers are injected from emitter into the base and the emitter current is zero. Under this condition the collector base junction J_C acts as a reverse biased diode and the Collector current I_C is equal to reverse Saturation Current -- (I_{CBO}) even though emitter current is zero.

Case:2 ∴ When the emitter base junction is forward biased and collector base junction is reverse biased the collector current will be

Let us Consider of n-p-n transistor. Electrons are injected to the base. These electrons constitute emitter current I_E. For example assume 100 electrons are injected into base region, Since the base is very thin very few of them say 2 in number, recombine with holes. This constitutes the base Current I_B. The remaining electrons, 98 in nos, Cross base collector reverse biased p-n function and appear on the collector side constituting the collector current I_C.

Thus the emitter current is always equal to

$$I_E = I_B + I_C$$

The base current is very small fraction of emitter Current, 2% or even loss than

The base current $I_B << I_C$,

$$\boxed{I_C = I_E}$$

ie the emitter current & collector current are nearly equal.

I_{CO} Reverse Saturation Current:

When emitter is open circuited, the base and the collector act as a reverse biased diode and the collector current I_C equals to reverse Saturation Current I_{CO}

$I_C = \alpha_{dc} I_E$ (1) by $I_C = \beta_{dc} I_B$

$I_C = \alpha_{dc}(I_C + I_B)$

$I_C = \alpha_{dc} I_C + \alpha_{dc} I_B$

$I_C - \alpha_{dc} I_C = \alpha_{dc} I_B$

$I_C(1 - \alpha_{dc}) = \alpha_{dc} I_B$

$$I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}}$$

almost all of I_E crosses to the collector unpn and only a small portion flows out of base terminal. Thatswhy 96% to 99.5% of I_E flows across the collector base junction to become the collector current.

$$I_C = \alpha_{dc} I_E$$

α_{dc} → emitter to collector current gain

β_{dc} → base to collector current gain

$\beta_{dc} I_C = \beta_{dc} I_B$

$$\frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} = \beta_{dc} I_B$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

W.K.T from $I_C = \beta_{dc} I_B \Rightarrow \beta_{dc} = I_C / I_B$

β_{dc} is known as common emitter dc current gain (h_{FE}). h_{FE} is the symbol used in transistor data sheets.

Pb Calculate I_E & I_C for a transistor has $\alpha_{dc} = 0.98$ $I_B = 100\,\mu A$. Determine β_{dc} (h_{FE}) for the transistor

I_E = Given $\alpha_{dc} = 0.98$

$I_B = 100\,\mu A$

To find

$\beta_{dc} = ?$.

W.K.T

$$I_C = \frac{\alpha_{dc} I_B}{1-\alpha_{dc}}$$

$$I_C = \frac{0.98 \times 100\,\mu A}{1-0.98} = 4.9\,mA$$

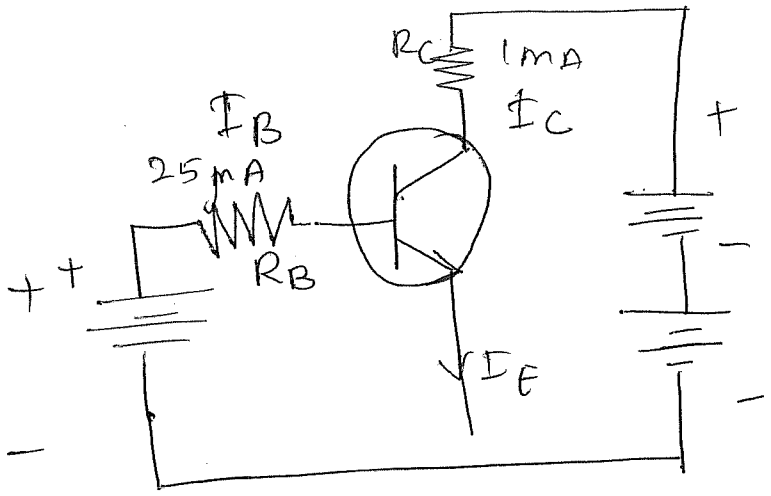
W.K.T

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{4.9\,mA}{0.98} = 5\,mA.$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.98}{1-0.98}$$

$$= 49.$$

Pb Calculate α_{dc} & β_{dc} for the transistor shown in figure. I_C is measured as 1 mA & $I_B = 25\,\mu A$. Determine the base current to give $I_C = 5\,mA$.



$$\beta_{dc} = \frac{I_C}{I_B} = \frac{1mA}{25\mu A} = 40$$

$$I_E = I_C + I_B$$

$$I_E = 1mA + 25\mu A.$$

$$= 1.025\ mA.$$

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{1mA}{1.025mA}$$

$$\alpha_{dc} = 0.976$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{5\ mA}{40}$$

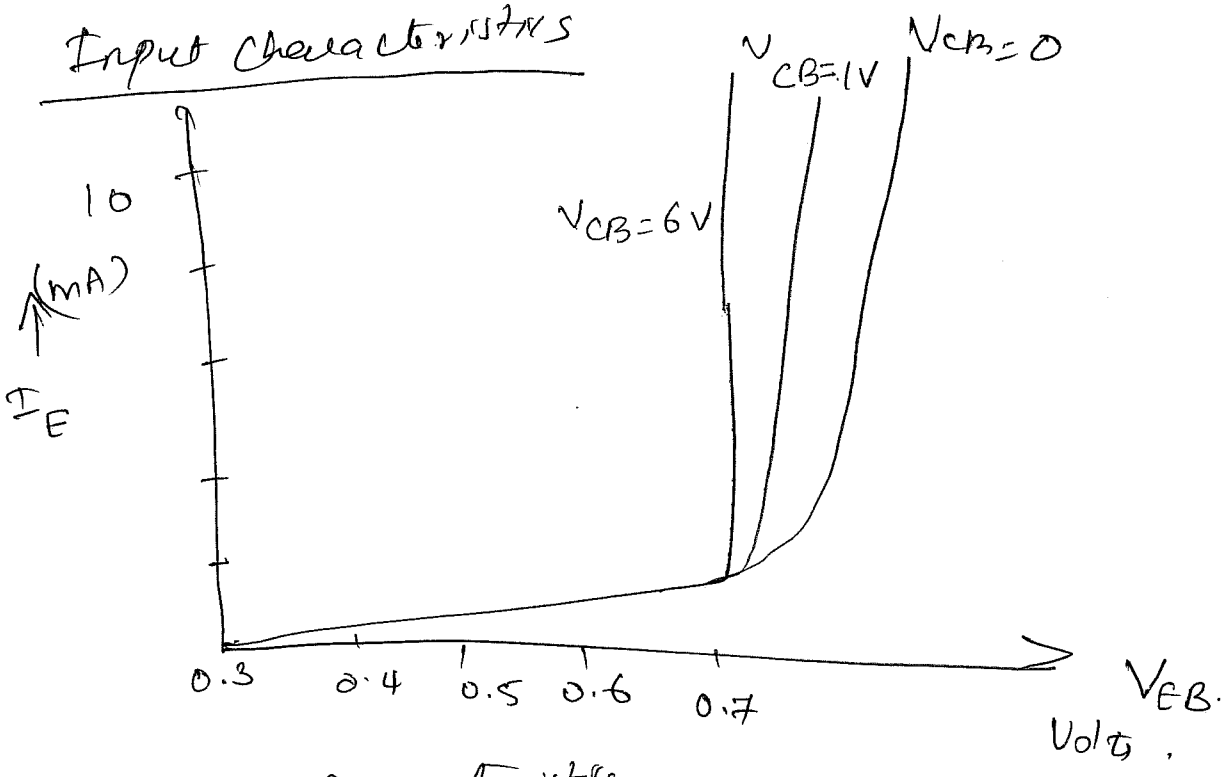
$$I_B = 125\ \mu A.$$

Transistor frequency response Characteristics

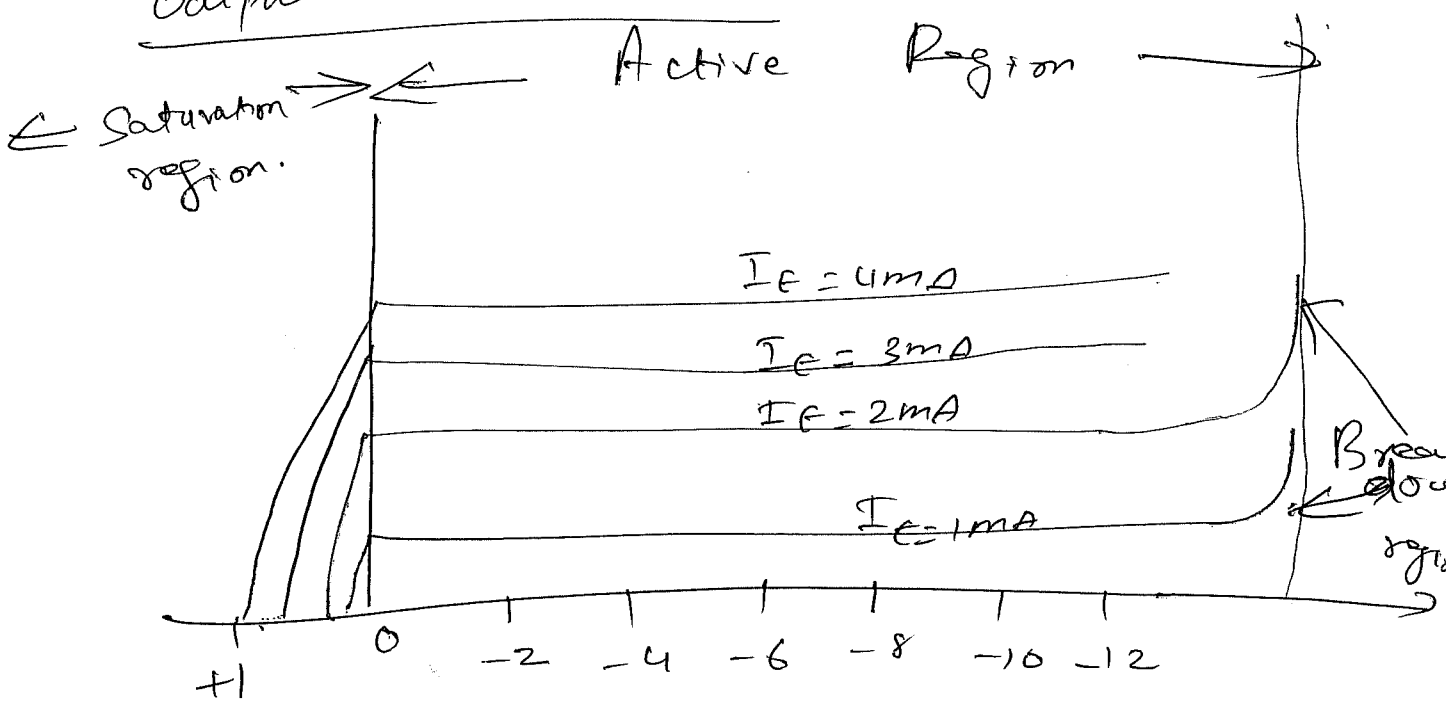
1. Common Base Characteristics
2. Common Emitter Characteristics
3. Common Collector Characteristics

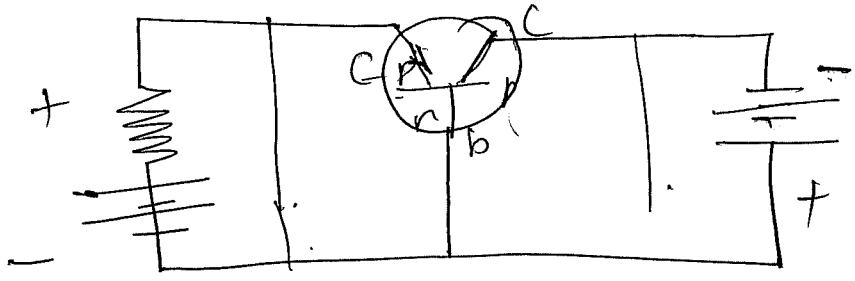
COMMON BASE CHARACTERISTICS

Input Characteristics



Output Characteristics

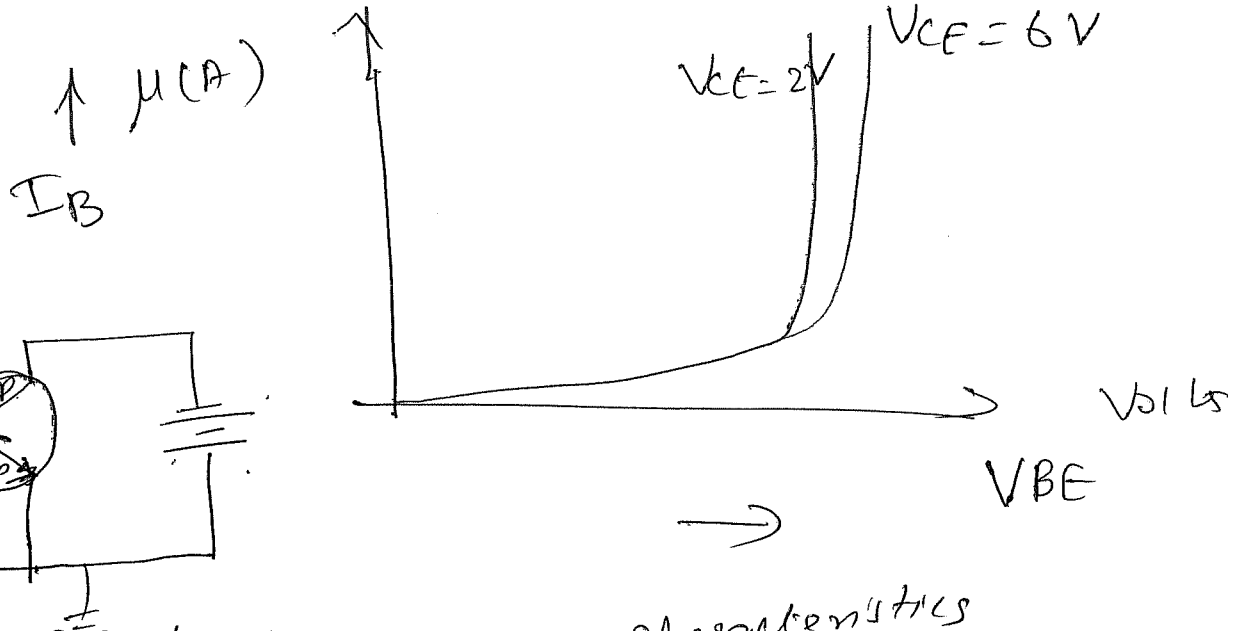




EB → Forward
BC → Reverse.

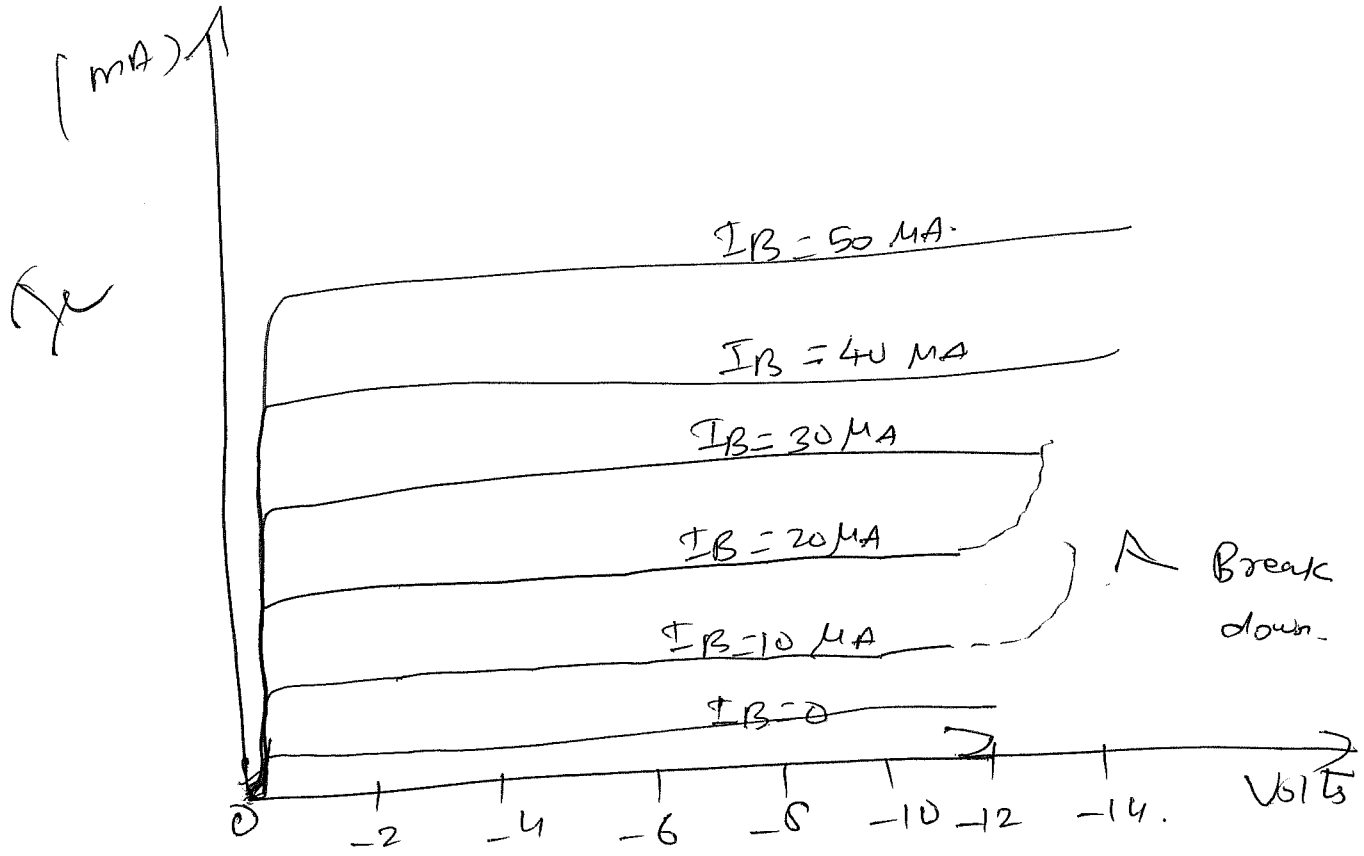
COMMON EMITTER CHARACTERISTICS

Input characteristics



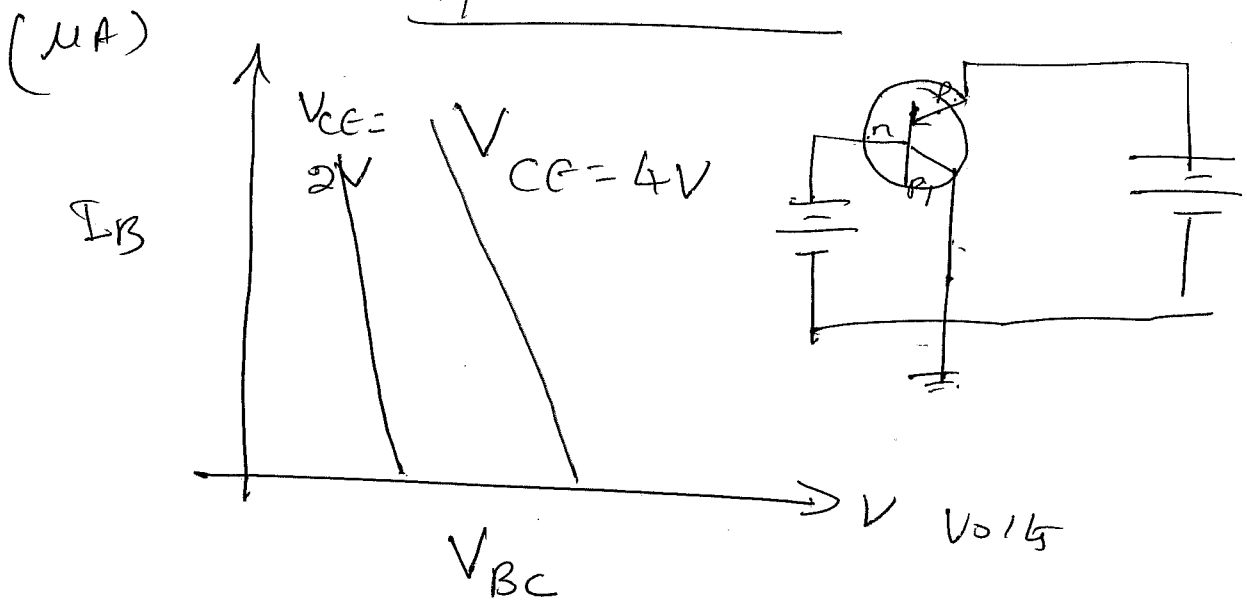
E–B → Forward
E–C → Reverse.

Output characteristics

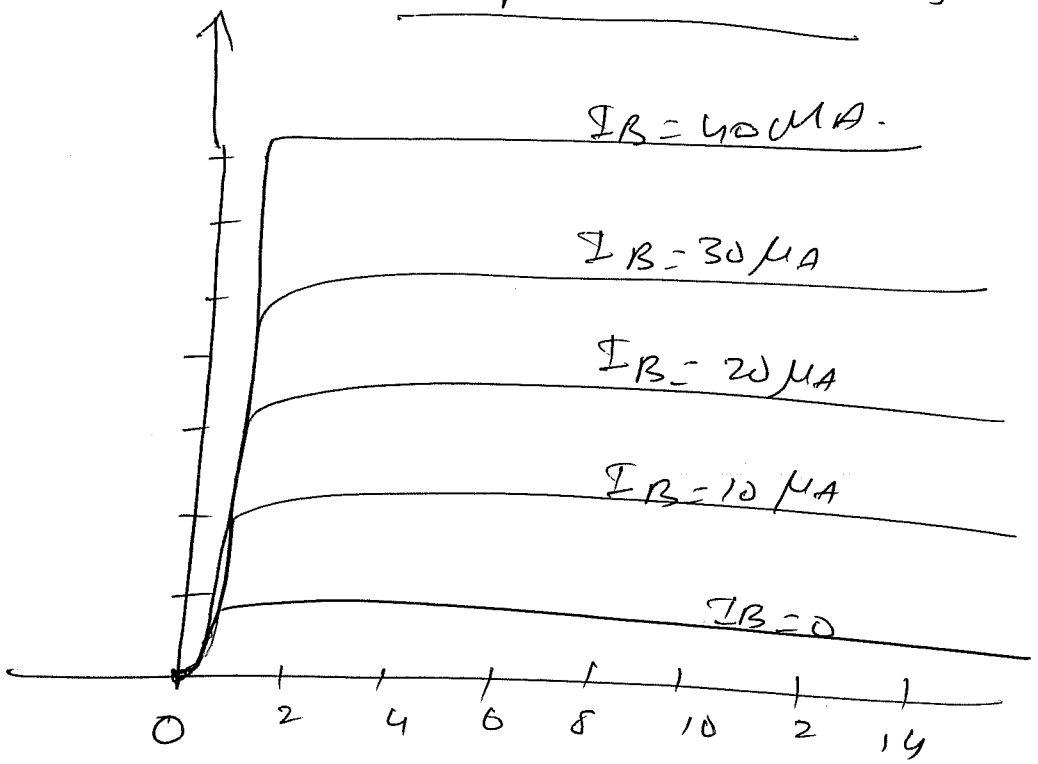


COMMON COLLECTOR CHARACTRISTICS CE Forward.
CB Reverse.

Input Characteristics



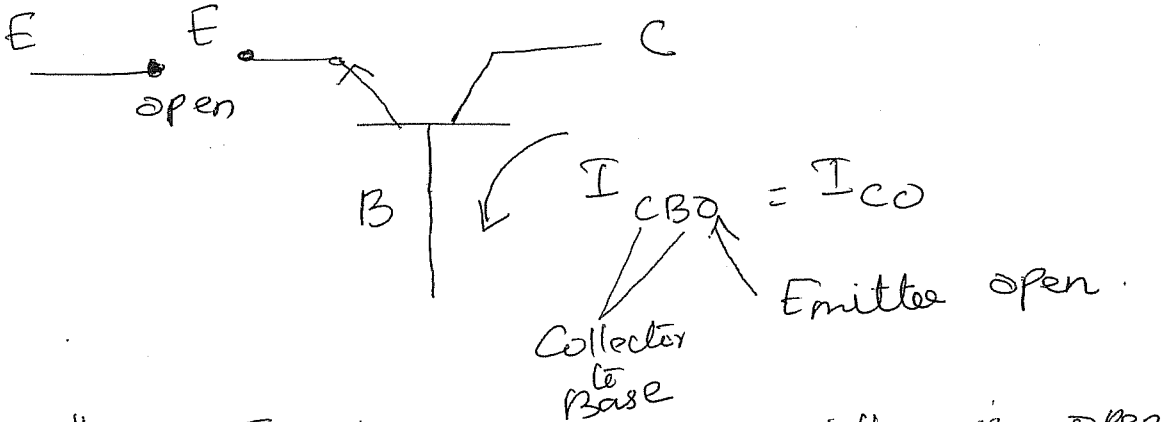
Output Characteristics



Alpha

1. In active region the base emitter junction is forward biased where as the collector base junction is reverse biased.
2. In the cut off region Base emitter junction and Collector - base junction both are reverse biased.
3. In the saturation region the base emitter and collector-base both are forward biased.

I_{CO} & I_{CBO}



* When I_E is Zero the emitter is open the Collector current is simply that due to the reverse saturation current I_{CO}. I_{CO} is very small in amplitude (micro amps).
* I_{CBO}, In general purpose transistors (especially using silicon) they may be low power, mid power and high power transistors. In case of high power transistors some reverse leakage current may be added. That reverse leakage current is known as I_{CBO}.

In dc mode levels I_C and I_E due to majority carriers are related by

$$\boxed{\alpha_{dc} = \frac{I_C}{I_E}} \quad \text{---(A)}$$

In general,

$$I_E = I_C + I_B. \quad \text{---(1)}$$

The collector current however comprises two components.

(i) due to majority carriers

(ii) due to minority carriers.

The minority-current components are called <u>leakage current</u> and is given by the symbol I_{CO}. (I_C current with emitter is open).

$$I_C = I_{C\,majority} + I_{CO\,minority}$$

$$I_C = I_c + I_{CBO} \quad \text{---(2)}$$

(A) $\Rightarrow$ $I_C = \alpha_{dc} I_E \Rightarrow I_C = \alpha I_E$

$$I_C = \alpha I_E + I_{CBO} \quad \text{---(3)}.$$

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \;\Big|\; V_{CB} = \text{constant}$$

$\alpha \rightarrow$ Common base, Short circuit, amplification factor.

Beta (β)

In the dc mode I_C and I_B are related by β.

α_{dc} = E–C Current gain

$$\beta_{dc} = \frac{I_C}{I_B} \quad \text{—①}$$

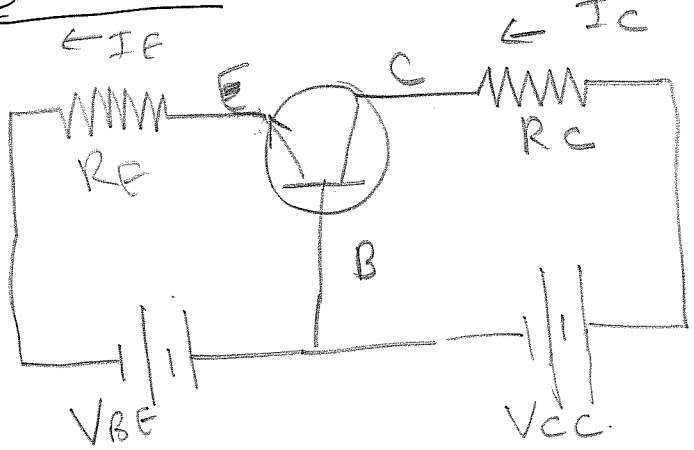
β_{dc} = B–C current gain

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big| V_{CE} = \text{Constant.}$$

$$I_C = \alpha_{dc} I_E$$
$$I_C = \beta_{dc} I_B$$

β_{ac} Common emitter, forward current amplification factor.

Common Base Configuration

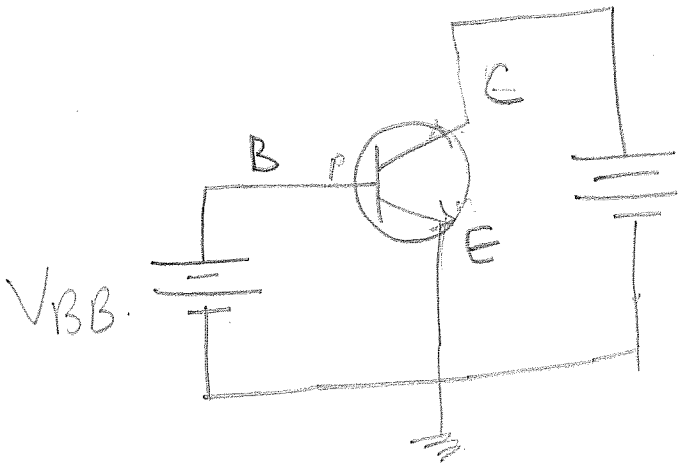


Emitter open

$$I_C = I_{C\,majority} + \frac{I_{C\,minority}}{(E\,open)}$$

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

Common Emitter configuration



Base open

$$I_C = I_{C\,maj} + I_{C\,minority}$$ B open.

$$I_C = \beta_{dc} I_B + I_{CEO}$$

Need for Biasing

Biasing is the process of applying external dc voltages of fixed or minimum magnitude to the two junctions of transistor. [EB & CB] to operate in the desired region.

The bipolar junction transistor can be operated in 3 regions by applying proper biasing. The 3 regions are

(i) cut off region (ii) Saturation region (iii) Active region.

Region	Junction EB	Junction CB	Application.
Cut off	Reverse Biased	Reverse Biased	Open Switch.
Active/Linear	Forward	Reverse	For proper Amplifier biasing.
Saturation	Forward	Forward.	Closed switch

a). Requirements of Biasing Circuit

* Biasing circuits are used to bias two junctions of a transistor.
* The circuit design should provide a degree of temperature stability.
* The operating Point should be made independent of transistors parameters such as β.

To satisfy the above requirement two techniques are normally used.

1. Stabilization Technique
2. Compensation Technique.

1 **Stabilization Technique:**

It refer to the use of resistor biasing circuit which allow I_B to vary, so as to keep I_C, the relatively constant with variations in I_{CBO}, β & V_{BE}

2. **Compensation Technique**

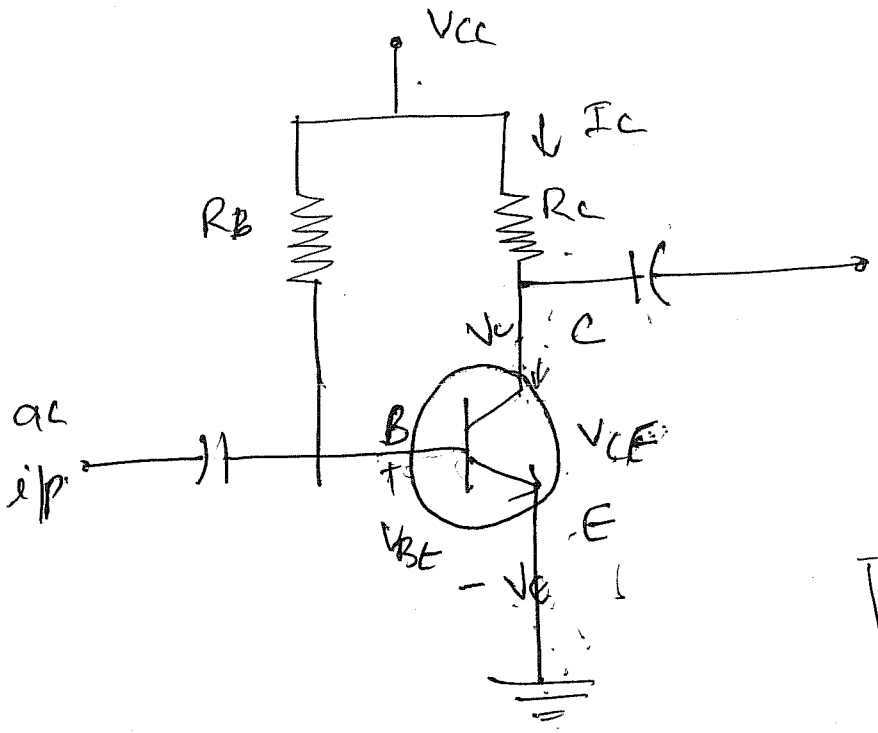
It refer to the use of temperature sensitive devices, such as diodes, transistor, Thermistor etc, which provide compensating voltages and current, to maintain Q point stable.

Operating Point

When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions, or The operating point is otherwise called as dc operating point or quiescent point or bias point.

- The operation point must be stable for the proper operation of the transistor
- But always it shifts with transistor parameters β, I_{CO}, V_{BE}. Operating point varies with temperatures because the transistor parameters are temp. dependent.

Fixed Bias Circuit.

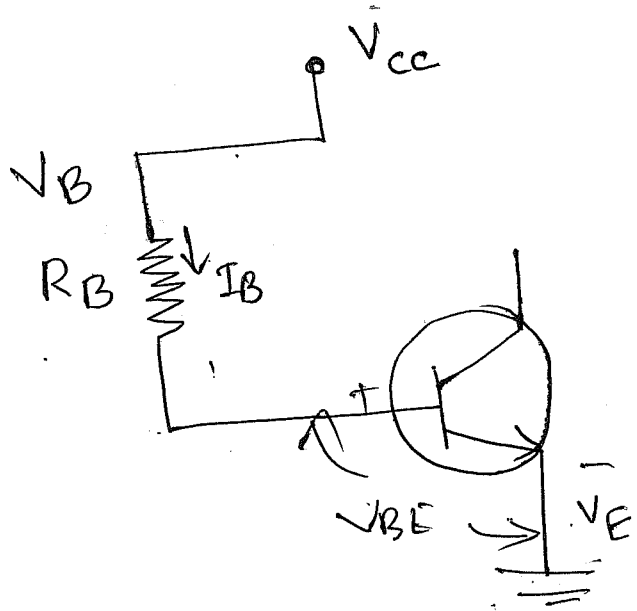


$$V_{CC} = V_{CE} + V_E$$

$$V_C = V_{CE} + V_E$$

$$\boxed{V_{CE} = V_C - V_E}$$

Base Circuit



$$V_B = + V_E = V_B$$

$$V_B = V_{BE} + V_E$$

$$\boxed{V_{BE} = V_B - V_E}$$

Applying Kirchoffs voltage Law to the base Circuit we get,

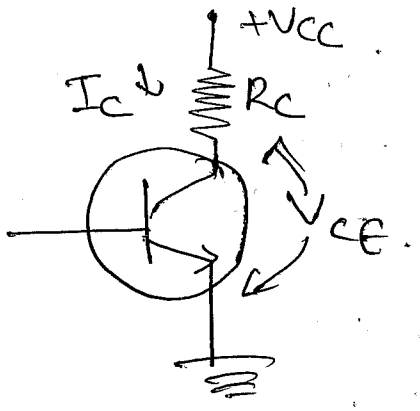
$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{cc} - V_{BE}$$

$$\boxed{I_B R = \frac{V_{cc} - V_{BE}}{R_B}}$$

Collector Circuit

Now we consider the Collector Circuit.



$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \beta I_B$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}}$$

It is important to note that base current is controlled by the value of R_B and I_C is related to I_B by β, and the magnitude of I_C is not a function of Resistance R_C.

w.k.t-

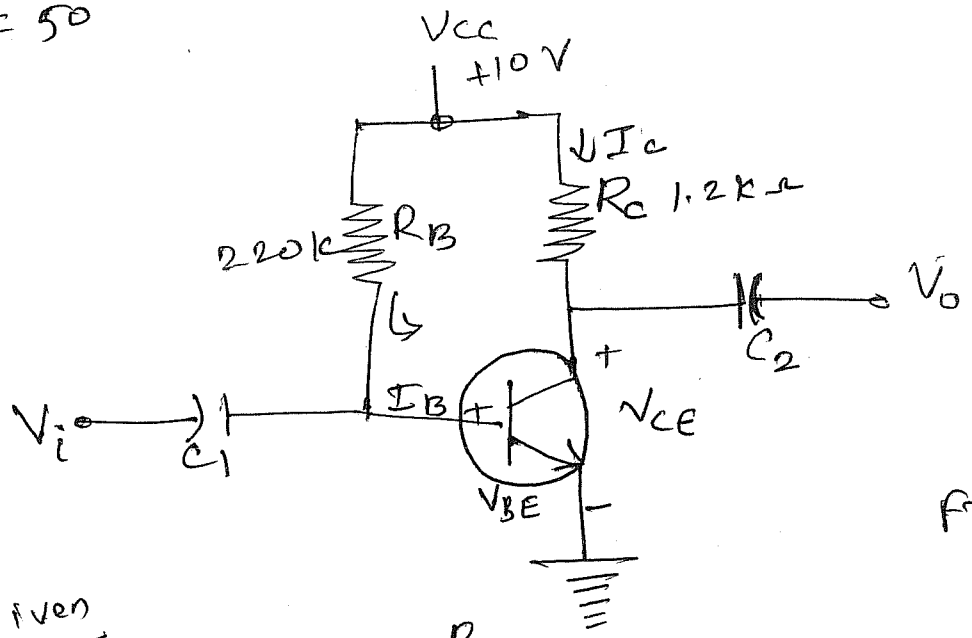
$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

In this circuit $V_E = 0$, Hence

$$\boxed{\begin{aligned} V_{CE} &= V_C \\ V_{BE} &= V_B \end{aligned}}$$

For the Circuit Shown in fig, Calculate $I_B, I_C, V_{CE}, V_B, V_C$ and V_{BC}. Assume $V_{BE} = 0.7V$, $\beta = 50$



Given

$V_{BE} = 0.7V$, $\beta = 50$

From the fig

$V_{cc} = +10V$

$R_B = 220K$

$R_c = 1.2\ K.$

To find

$I_B, I_C, V_{CE}, V_B, V_C.$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{10V - 0.7V}{220\ K} = \frac{10V - 0.7V}{220 \times 10^{+3}}$$

$$\frac{9.3}{220000} = 0.042272 \times 10^{-3}$$

$$= 42.272\ \mu A$$

4.2272×10^{-5}

$\frac{4.2272 \times 10}{10} \times 10^{-5}$

$4.2272 \times 10 \times \frac{10^{-5}}{10}$

$4.2272 \times 10 \times 10^{-6}$

42.272×10^{-6}

$I_B = 42.272\ \mu A.$

$$I_C = \frac{V_{cc} - V_{CE}}{R_c}$$

$$= 10V$$

$I_C = \beta I_B.$

$I_C = 50 \times 42.27 \times 10^{-6}$

$I_c = 2.1135 \times 10^{-6}$

$I_c = 2.113 \times 10^{-3}$

$\boxed{I_c = 2.113\ mA}$

$V_{CE} = V_{CC} - I_C R_C$

$= 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^{3}$

$= 10 - 2.532$

$\boxed{V_{CE} = 7.468\ V}$

$V_B = V_{BE} = 0.7\ V$

$V_C = V_{CE} = 7.468\ V$

$V_{BC} = V_B - V_C = 0.7 - 7.468$

$= -6.7638\ V.$

Calculate the minimum and maximum values of I_C and V_{CE} for the base bias when $h_{FE(min)} = 50$ and $h_{FE\,max} = 60$. For Circuit $V_{CC} = 12\ V$, $R_C = 2K$ and $R_B = 150\ K$. Assume Silicon transistor.

Soln

Given

$h_{FE(min)} = 50$ & $h_{FE(max)} = 60$,

$V_{CC} = 12\ V$

$R_C = 2\ K$, $R_B = 150K$, For Silicon Transistor $V_{BE} = 0.7\ V$

To find

The minimum and maximum values of I_C and V_{CE}.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12V - 0.7V}{150\ K} = \frac{11.3}{150 \times 10^3}$$

$$I_B = 75.33\ \mu A.$$

(i) for $h_{FE(min)}$ $[\beta_{min}]$

$$I_C = h_{FE(min)} \times I_B$$

$$= 50 \times 75.33\ \mu A.$$

$$= 3.766 \times 10^{-3}$$

$$h_{FE(min)} = 3.766\ mA$$

(ii) For $h_{FE(MAX)}$ $[\beta_{max}]$

$$I_C = h_{FE(max)} \times I_B$$

$= 60 \times 75.33\ \mu A.$

$h_{FE} = 4.52\ mA.$

$V_{CE} = V_{cc} - I_c R_c$ [Sub I_c for h_{FE} min]

$= 12 - \frac{3.766 \times 10^{-3}}{h_{FE\ min}} \times 2 \times 10^{3}$

$V_{CE} = 4.46\ V$ [h_{FE} min]

$V_{CE} = V_{cc} - I_c R_c$ Sub I_c for h_{FE} max.

$= 12 - 4.52\ mA \times 2 \times 10^{3}$

$= 12 - 4.52 \times 10^{-3} \times 2 \times 10^{3}$

$= 3V.$

$V_{CC} - I_c R_c - V_{CE} = 0$

$V_{CE} = V_{CC} - I_c R_c$

Ans

h_{FE} min, $I_c = 3.767\ mA.$

$V_{CE} = 4.466\ V$

h_{FE} max $I_c = 4.52\ mA$

$V_{CE} = 3\ V$

$I_B = 75.33\ \mu A.$

Types of Bias circuits

1) Fixed Bias Circuit
2) ~~Emitter~~ Collector to Base Bias ckt
3) Voltage divider Bias
4) Emitter stabilized Bias

DC and AC load line

For fixed bias Circuit, we have

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

$$= \frac{V_{CC}}{R_C} - \left[\frac{1}{R_C}\right] V_{CE}$$

(1) For point A
$V_{CE} = V_{CC}$

(2) For point B
$V_{CE} = 0$

$$I_C = -\left[\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C}$$

$$y = m x + c$$

By comparing this equation with equation of straight line $y = mx + c$

Where $m \rightarrow$ Slope
$c \rightarrow$ Intercept on y axis.

We can draw a straight line on graph of I_C Vs V_{CE} which is having slope $-1/R_C$. and y intercept V_{CC}/R_C.

To determine the two points on the line we assume $V_{CE} = V_{CC}$, & $V_{CE} = 0$

i) When $V_{CE} = V_{CC}$, $I_C = 0$,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad [\text{if } V_{CE} = V_{CC}]$$

$$I_C = \frac{V_{CC} - V_{CC}}{R_C}$$

$I_C = 0 \Rightarrow$ and we get point A.

(iii) When $V_{CE} = 0$,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$ Sub $V_{CE} = 0$ in this eqn,

$$I_C = \frac{V_{CC} - 0}{R_C}$$

$$\boxed{I_C = \frac{V_{CC}}{R_C}} \Rightarrow$$ and we get Point B.

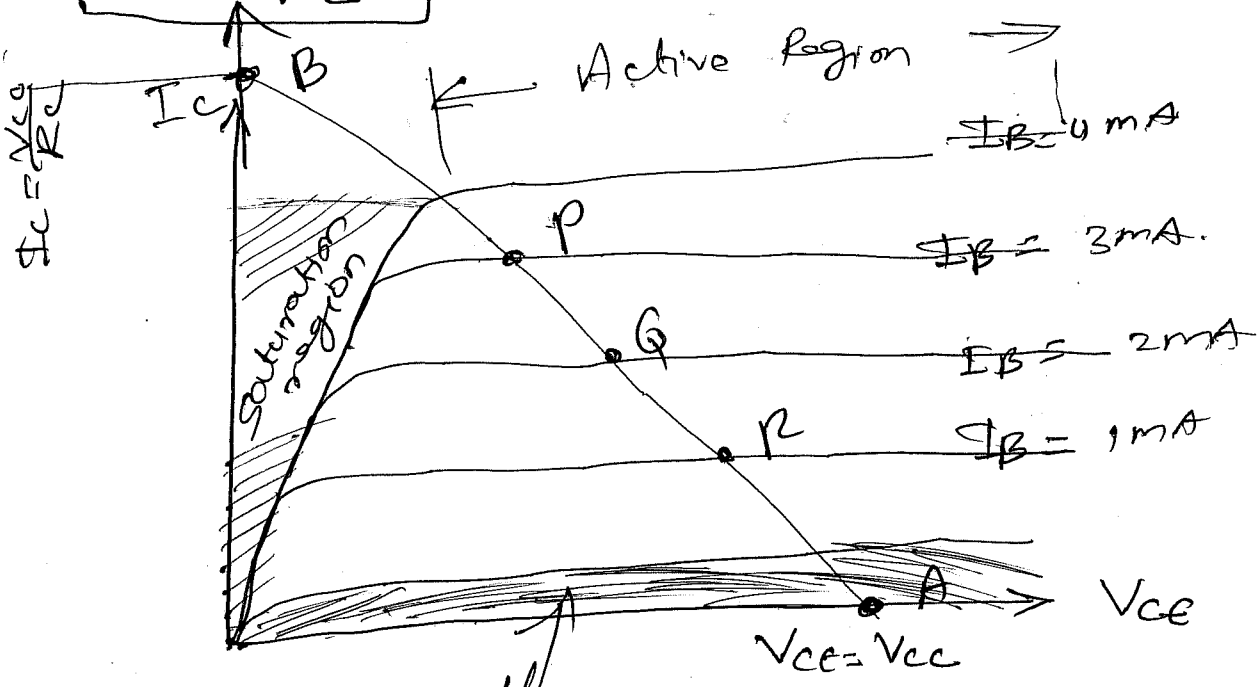


Fig. Common emitter output characteristics with dc load line.

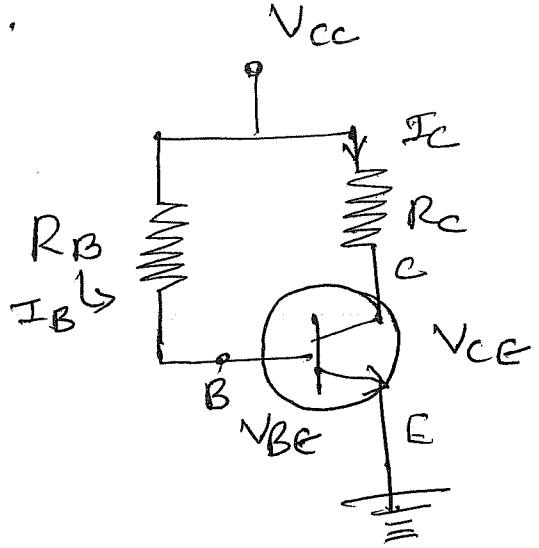
The dc load line is a plot of I_C versus V_{CE} for a given value of R_C and V_{CC}. Thus it represents all collector current levels and corresponding collector emitter voltages that can exist in the circuit.

Knowing any one of I_C, I_B or V_{CE} it is easy to determine other two from

the load line. The slope of the dc load line depends on the value of R_c.

$$m = -\left[\frac{1}{R_c}\right] V_{cc}.$$

Its negative and equal to reciprocal of R_c.



$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{cc} - V_{BE}.$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

C.W.K.T.

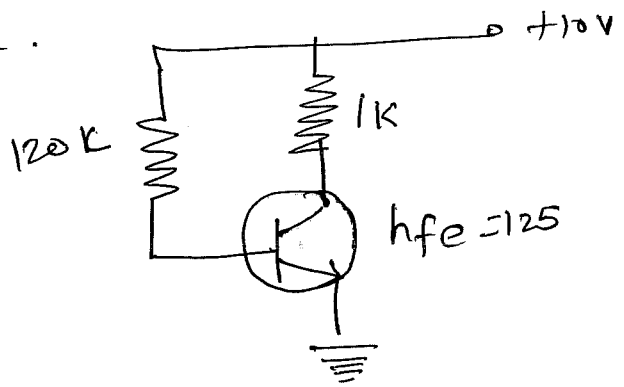
The intersection of curves of different values of I_B with dc load line gives different operating points. From different values of I_B we get different intersection points, (quiescent Points or Q Point) such as P, Q, R.

Choosing the Operating Point

* Transistor functions most linearly when it is constrained to operate in its active region.
* To establish an operating point in this region it is necessary to provide appropriate proper voltages and currents using external sources.
* The importance of selecting an operating point of a CE transistor amplifier is, It should be in its active region of output characteristics.

*

Pb Draw a DC load line of the circuit shown in figure.



Step:1 Obtain I_{CQ}, V_{CEQ} Poi for point A & B.

Applying KVL,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{10 - 0.7}{120k} = 77.5\ \mu A.$$

To find I_{CQ}, ($h_{fe} = \beta$)

Relationship between I_C & β is

$$I_{CQ} = \beta I_B$$

$$= 125 \times 77.5\ \mu A$$

$$\boxed{I_{CQ} = 9.6875\ mA.}$$

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CEQ} = 0$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$V_{CEQ} = 10 - 9.6875mA \times 1k$$

$$\boxed{V_{CEQ} = 0.3125V}$$

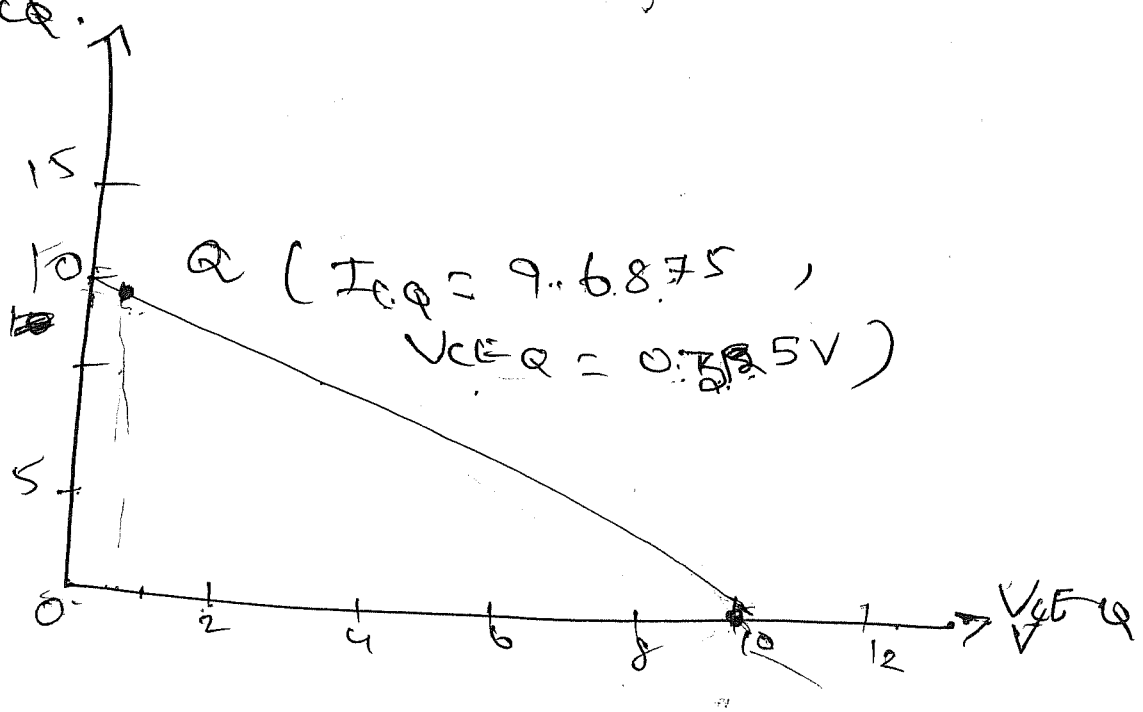
Step: 2

Mark axis intersection points,

Point A : $V_{CE} = V_{CC} = 10V$ at $I_C = 0$

Point B $I_C = \frac{V_{CC}}{R_{dc}} = \frac{V_{CC}}{R_C} = \frac{10}{1k} = 10mA$

Step: 3 Draw the Load line.



Why CE Configuration is widely used.

✓ CE Configuration is widely used because CE is the only Configuration which provides both voltage gain and current gain greater than Unity.

in CB Curren gain is less than Unity

in CC Voltage gain is less than Unit.

✓ The power of the CE amplifier is much greater than the power gain provided by the other two configurations.

Need of Biasing

- The transistor can be operated into 3 regions. (i) Saturation (ii) Cut-off and (iii) Active.

To operate the transistor in the desired region we have to apply external dc voltages of current polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor. Because dc voltages are used to bias the transistor the biasing is known as dc biasing.

Operating Point:

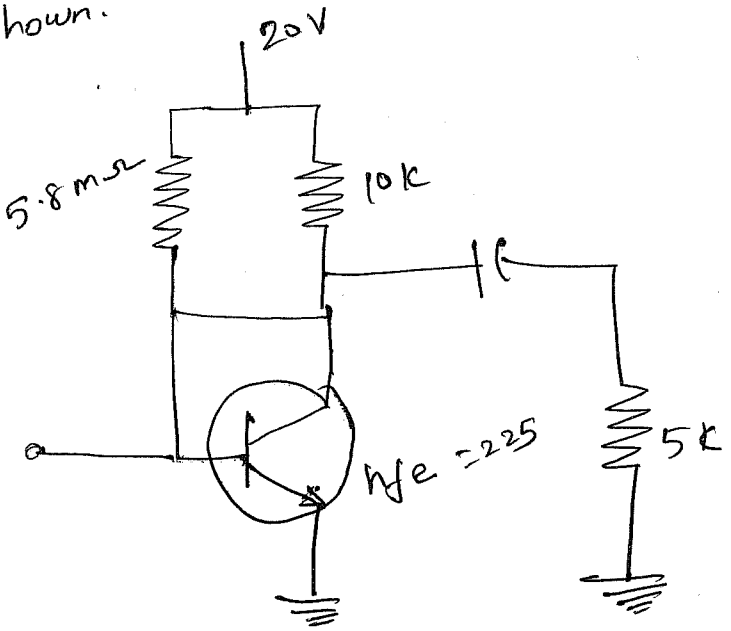
When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are called the Operating conditions or dc Operating point or quiescent point or bias point.

The Operating point must be stable for proper operation of the transistor. However the operating point shifts with changes in transistor parameters, such as β, I_{CO} & V_{BE}.

✓ As transistor parameters are temperature dependent the operating point also varies with changes in temperature.

Pb

Locate the dc operating point of the circuit shown.



Soln

Since the base emitter junction is not reverse biased, we can say that the transistor is not in cut off region. Hence assume that the transistor is operating in active region.

Applying KVL, to the base loop,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} = V_{BE} + I_B R_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{5 \times 10^6} = 3.327\ \mu A$$

In active region

$$I_C = \beta I_B$$

$$I_C = 225 \times 3.327 \times 10^{-6}$$

$$I_C = 0.7487\ mA.$$

Now applying KVL to the collector loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 20 - 0.7487 \times 10^{-3} \times 10 \times 10^3$$

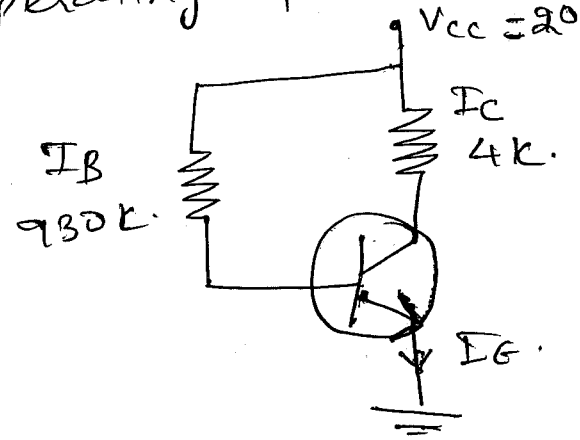
$$V_{CE} = 12.5\ V$$

Since $V_{CE} = 12.5$ V collector to base junction is reverse biased

$$I_{CQ} = 0.7487\ mA. \quad \checkmark$$

$$V_{CEQ} = 12.5\ V. \quad \checkmark$$

Pb For the circuit shown in fig, determine the operating points with $\beta = 100$.



KVL

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{930 \times 10^3} = 10\ \mu A.$$

In active region,

$$I_C = \beta I_B$$

$$I_C = 100 \times 10\ \mu A$$

$$I_C = 1\ mA.$$

Apply KVL to the collector loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 20 - (1 \times 10^{-3})(4 \times 10^3) = 16V$$

Since $V_{CE} = 16V$, the collector to base junction is reverse biased, and we say that our assumption that transistor is in active region is justified. Therefore Q point or operating point is at

$$V_{CEQ} = 16V$$

$$I_{CQ} = 1mA.$$

SELECTION OF OPERATING POINT

The operating point can be selected at different positions on the dc load line. They are

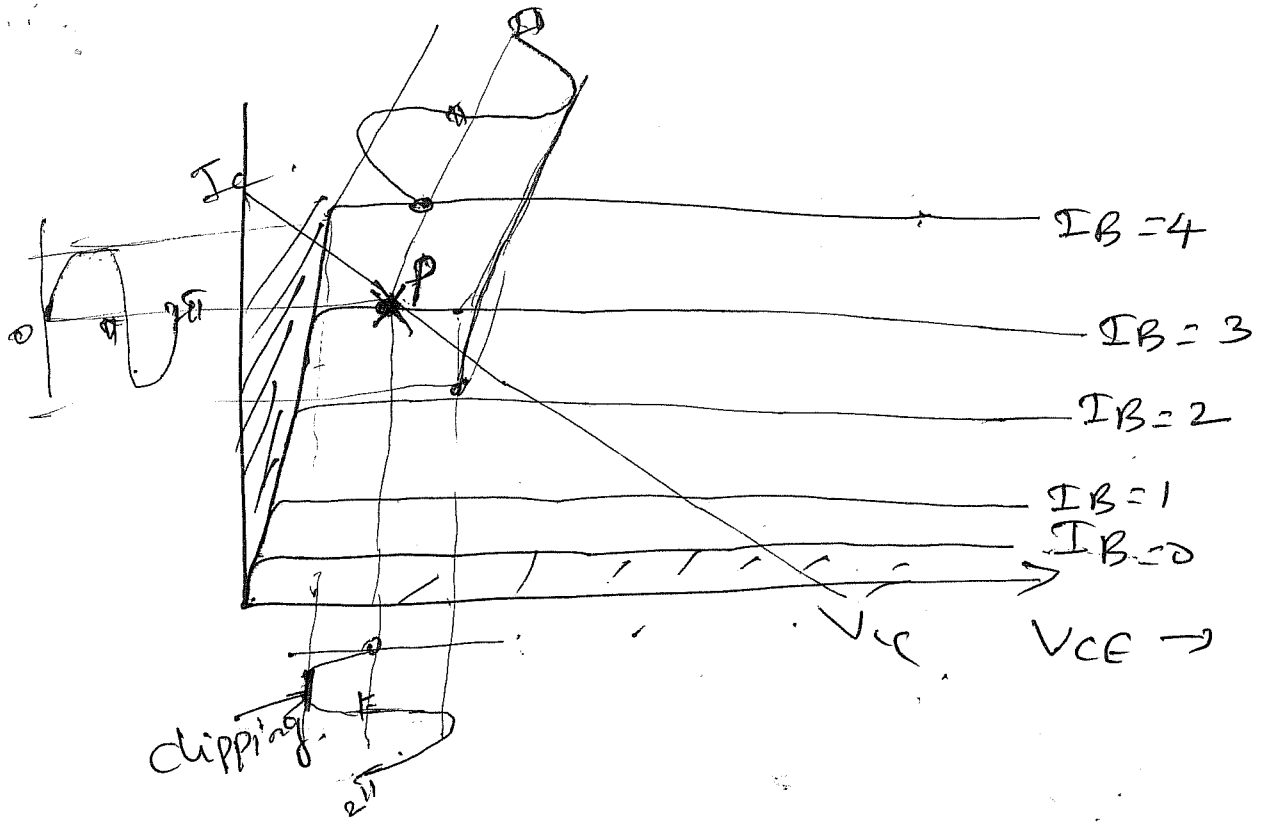
(i) Near Saturation Region
(ii) Near cut off Region
(iii) At the center (in Active Region)

The selection of operating Point will depend on its application.

When transistor is used as an amplifier the Q point should be selected at the centre of DC load line to prevent any possible distortion in the amplified signal.

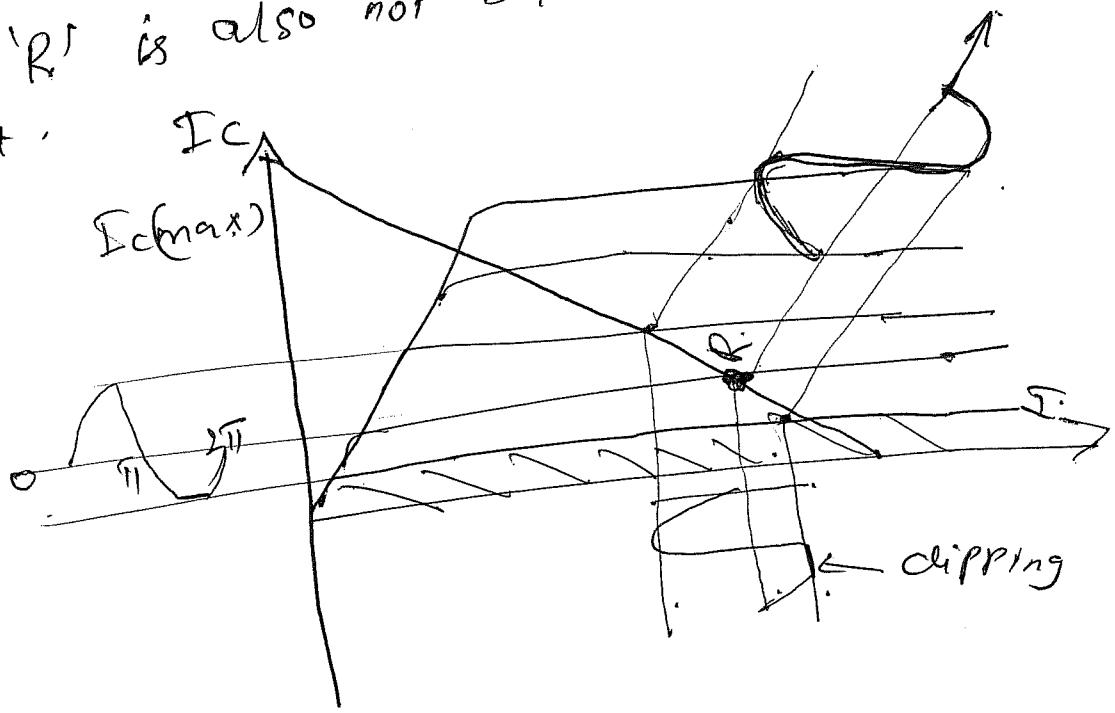
Case : 1 (Near Saturation Region)

Biasing Circuit is designed to fix a Q point at point P. Point P is very near to the Saturation region. In this region Collector current is clipped at the positive half cycle. Eventhough base current Varies Sinusoidally Collector Current is clipped at the positive half cycle. So even base current Varies sinusoidally Collector current is a not a useful sinusoidal waveform - (i.e) distortion is present at the output. i.e P is not a suitable operating point.



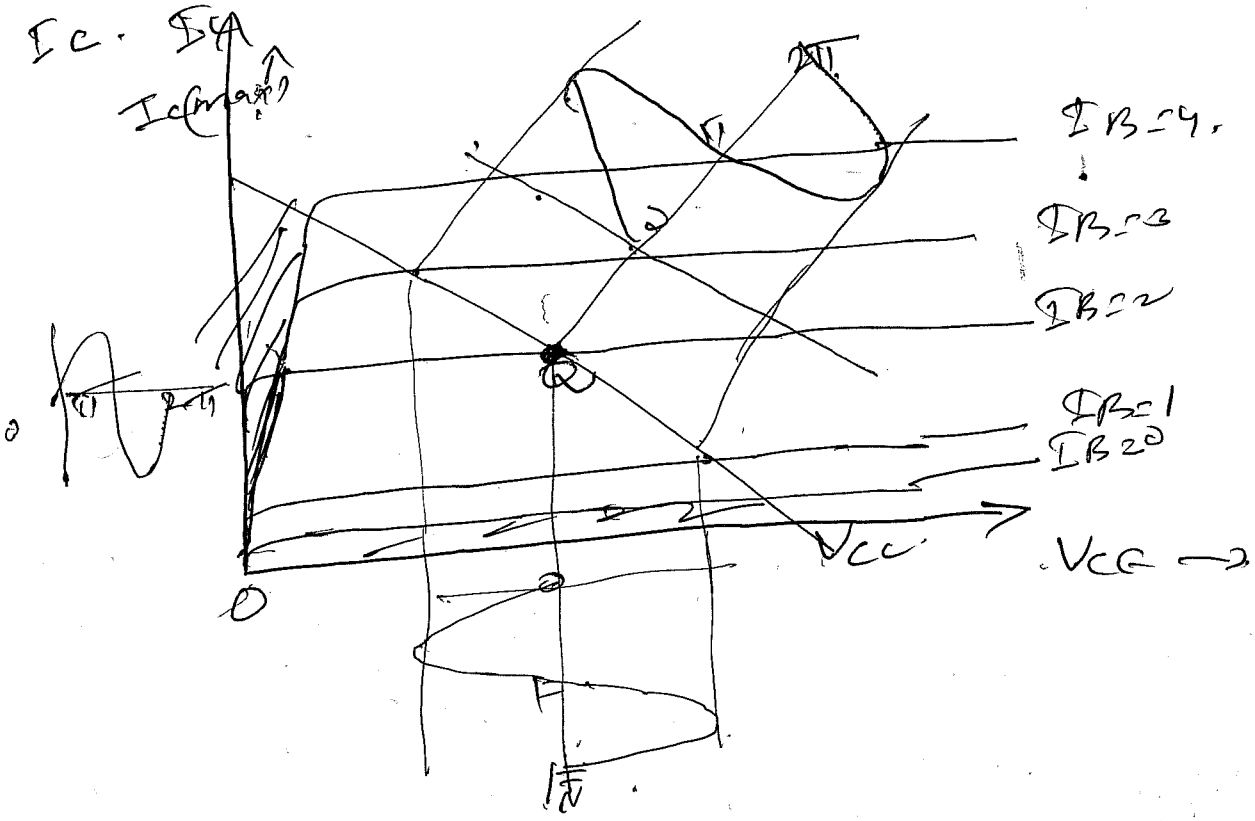
Case: 2

Biasing Circuit is designed to fix a Q point at R is shown in fig. Point R is very near to cut-off. The collector current is clipped at the negative half cycle. So Point 'R' is also not suitable operating point.



Case: 3

Biasing circuit is designed to fix a Q point. The Q point signal is Sinusoidal waveform without any distortion. Thus the point Q is best operating point.



In an N-P-N transistor base grounded.

$I_C = \alpha I_E$

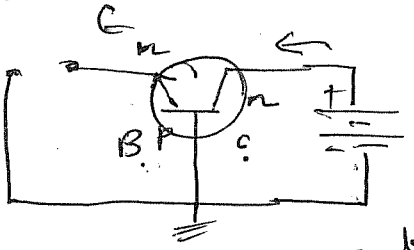
The collector current is the current due to majority and minority carriers.

I_{CBO}

$I_C = I_{Cmajority} + I_{Cminority}$

$I_C = I_{Cmaj} + I_{Cmin}$

$I_C = \alpha I_E + I_{Cmin}$



$$\boxed{I_C = \alpha I_E + I_{CBO}}$$

I_{CBO} → Reverse saturation collector current due to minority carriers when emitter is open.

$I_C = \alpha I_E + I_{CBO}$

But WKT, $I_E = I_C + I_B$

$I_C = \alpha(I_C + I_B) + I_{CBO}$

$I_C = \alpha I_C + \alpha I_B + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

$I_C(1-\alpha) = \alpha I_B + I_{CBO}$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}} \Rightarrow$$

$$\boxed{I_C = \beta I_B + (\beta+1) I_{CBO}}$$

Relation ship between α & β

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1$$

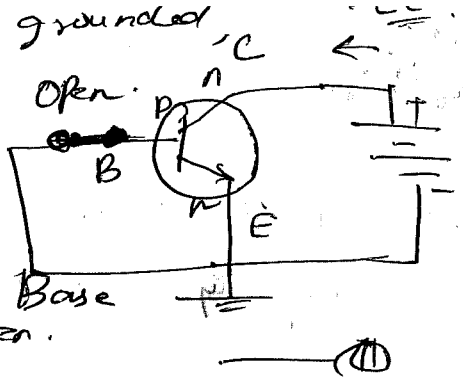
$$\beta + 1 = \frac{\alpha + (1-\alpha)}{1-\alpha}$$

$$= \frac{\alpha + 1 - \alpha}{1-\alpha}$$

$$\boxed{\beta + 1 = \frac{1}{1-\alpha}}$$

$I_{CBO} =$

In an n-p-n transistor Base grounded,



$I_C = I_{majority} + I_{minority}$

$$I_C = \beta I_B + I_{CEO}$$ when Base is open. —(1)

$I_C = \beta I_B + I_{CEO}$

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$ when Emitter is open. —(2)

O

STABILITY FACTORS

To maintain the operating point stable by keeping I_C and V_{CE} constant, so that the transistor will work in a active region. Stabilization techniques and compensation techniques are normally used to maintain the operating point stable.

In order to compare the stability provided by these circuits one term is raised called stability factor, which indicates degree of change in operating point due to variation in temperature.

Since there are three variables which are temperature dependent, the stability factors are,

(i) $S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\beta\ const}$ (or) $S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\beta const.}$

(ii) $S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta\ const}$ (or) $S' = \left.\frac{\Delta I_C}{\partial V_{BE}}\right|_{I_{CO},\beta const.}$

(iii) $S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},V_{BE}\ const}$ or $S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},V_{BE}\ Const.}$

Stability factor (S)

The collector current however comprises two components.

(i) Due to majority carriers.
(ii) Due to minority carriers.

The minority components are called leakage current.

and it is given by I_{CEO} i.e the I_C current when emitter is open.

I_C = I_C marority + I_{CO} minority $\quad I_C = \beta I_B$

$I_C = I_C + I_{CEO}$

$I_C = \beta I_B + I_{CEO}$ w.k.t

STABILITY FACTOR

$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad \text{——(1)}$$

When I_{CBO} for a open based transistor the minority current carriers are I_{CEO}. The collector current is

$I_C = I_{Cmax} + I_{Cmin}$

$I_C = \beta I_B + I_{CEO}$ ——(2).

Equating (1) & (2),

$I_{CEO} = (1+\beta) I_{CBO}$.

when I_{CBO} changes by ∂I_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C. So this (1) equation becomes,

$$\partial I_C = \beta \partial I_B + (1+\beta) \partial I_{CBO} \quad \text{——(3)}$$

$\frac{\partial}{\partial}$ the equation (3) by ∂I_C

$$\frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}.$$

$$(1+\beta)\frac{\partial I_{CBO}}{\partial I_C} = 1-\beta\ \frac{\partial I_B}{\partial I_C}$$

$$\frac{\partial I_{CBO}}{\partial I_C} = \frac{(1-\beta)\ \frac{\partial I_B}{\partial I_C}}{1+\beta} \quad \text{——(4)}$$

but $S = \frac{\partial I_C}{\partial I_{CBO}}$, Inverting (4), $\frac{\partial I_C}{\partial I_{CBO}}$

$$\frac{\partial I_C}{\partial I_{CBO}} = S = \frac{1+\beta}{(1-\beta)\frac{\partial I_B}{\partial I_C}}.$$

$$\boxed{S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}} \quad \text{——(5)}$$

The above equation can be considered as a standard equation for derivation of stability factors of other biasing circuits.

STABILITY FACTOR FOR FIXED BIAS CIRCUIT

From a fixed bias circuit,

$$I_B = \frac{V_{CC}}{R_B}. \quad \text{——(6)}$$

In the above equation I_B changes by ∂I_B V_{CC} and V_{BE} are not affected. Partiall diff w.r.t I_C (6), $\Rightarrow \frac{\partial I_B}{\partial I_C} = 0$ (coz I_C not present in the equation),

w.k.t,

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

now sub $\partial I_B/\partial I_C = 0$ in this above equation,

$$S = \frac{1+\beta}{1-\beta(0)} \Rightarrow \frac{1+\beta}{1}$$

$$\boxed{S = 1+\beta} \leftarrow \text{fixed bias Circuit.}$$

Stability Factor S'

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big| \; I_{CO}, \beta \text{ constant.}$$

we have, I_C is

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

Now representing I_B in terms of V_{BE} we get,

w.k.t $I_B = \frac{V_{CC} - V_{BE}}{R_B}$, substituting

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (\beta+1)\, I_{CBO}$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CBO} \quad \text{---(7)}$$

partial diff (7) w.r.t V_{BE}

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B}$$

$$\boxed{S' = \frac{-\beta}{R_B}}$$

Stability factor S''

$$S'' = \frac{\partial I_C}{\partial \beta} \Big| V_{BE}, I_{CO} \text{ constant.}$$

We have, I_C as

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CBO},$$

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_B} + \frac{V_{BE}}{R_B} + I_{CBO}$$

$$= \left(\frac{V_{CC}}{R_B} + \frac{V_{BE}}{R_B}\right) + I_{CBO}$$

$$\frac{\partial I_C}{\partial \beta} = I_B + I_{CBO} \quad \text{---(8)}$$

$I_C = \beta I_B$

$I_B = \frac{I_C}{\beta}$

$V_{CC} - V_B - V_{CE} = 0$

$V_{CC} - V_{CE} = V_B$ in terms of I,

$\left(\frac{V_{CC}}{R_b} - \frac{V_{CE}}{R_b}\right) = \frac{V_B}{R_B}$

$I_B = \frac{V_{CC}}{R_B} - \frac{V_{CE}}{R_B}$

w.k.t, $I_C = \beta I_B + I_{CEO}$

$I_C = \beta I_B + I_{CEO}$

$\div \beta$

$\frac{I_C}{\beta} = I_B + \frac{I_{CEO}}{\beta}$

$\frac{I_C}{\beta} = I_B + \frac{I_{CEO}}{\beta}$

as I_{CEO} is very little while comparing with I_B it can be eliminated.

$$\frac{I_C}{\beta} = I_B + \frac{I_{CEO}}{\beta}$$

$$I_B = \frac{I_C}{\beta}$$

(8) $\Rightarrow$

$$\frac{\partial I_C}{\partial \beta} = I_B$$

[I_{CBO} can be less and neglected.

$$S' = \boxed{\frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}}$$

[I_B in terms of β neglecting reverse saturation]

where $I_B = \frac{I_C}{\beta}$

Relation Between S and S'

$$S = 1+\beta$$

$$S' = \frac{-\beta}{R_B}$$

x lying & ÷ ing numerator by $1+\beta$

$$S' = \frac{-\beta(1+\beta)}{R_B(1+\beta)}$$

$$\boxed{S' = \frac{-\beta S}{R_B(1+\beta)}} \qquad \therefore S = 1+\beta$$

Relation between S and S''

$$S = 1+\beta$$

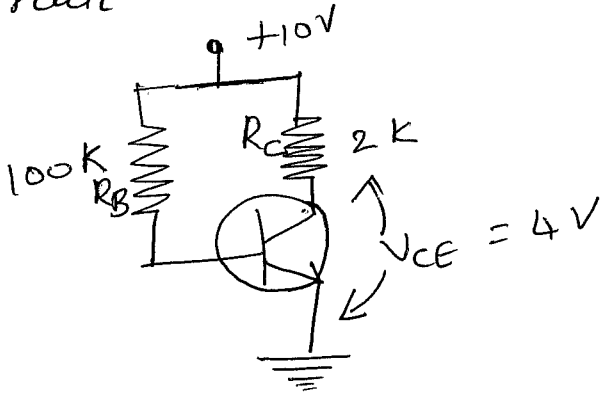
$$S'' = \frac{I_C}{\beta}$$

x by and ÷ numerator and denominator by $(1+\beta)$

$$S'' = \frac{I_C(1+\beta)}{\beta(1+\beta)}$$

$$\boxed{S'' = \frac{I_C S}{\beta(1+\beta)}}$$

Pb In the circuit shown in fig calculate 'S'.



Soln

The Circuit shown is a fixed bias circuit. The Stability factor is

$$S = 1 + \beta.$$

To find β we should Calculate I_B & I_C.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{10 - 4}{2 \times 10^3} = 3\,mA.$$

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{100 \times 10^3} = 93\,\mu A$$

$$\beta = \frac{I_C}{I_B} = \frac{3 \times 10^{-3}}{93 \times 10^{-6}} = 32.258$$

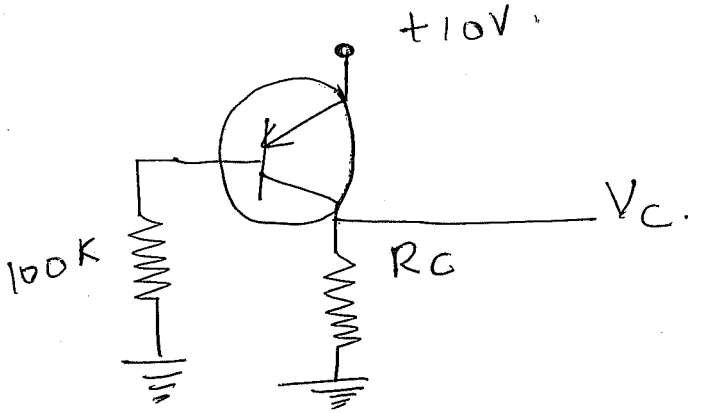
The Stability factor,

$$S = 1 + \beta = 1 + 32.258$$

$$\boxed{S = 33.258}$$

---

b/ For the Pnp transistor shown $\beta = 50$. Find the values of R_C to obtain $V_C = 5V$. what happens if the transistor is replaced with another $\beta = 100$.



To find
$R_C = ?$

Given
$V_C = 5V$

If $\beta = 100$ what is R_C.

V_{BE}: $V_{CC} - V_{BE} - I_B R_B = 0$

$V_{BE} = V_{CC} - V_{BE} - V_B = 0$

$V_B = V_{CC} - V_{BE} = 10 - 0.7 = 9.3V$

$V_B = 9.3V$

$I_B * R_B = V_B$

$I_B = \frac{V_B}{R_B} = \frac{9.3V}{100K} = 93\ \mu A.$

for $\beta = 50$,

$I_C = \beta I_B = 50 \times 93\ \mu A$

$I_C = 4.65\ mA.$

$R_C = \frac{V_C}{I_C} = \frac{5V}{4.65mA} = 1075\ \Omega$

For $\beta = 100$,

$I_C = \beta I_B = 100 \times 93\ \mu A = 9.3\ mA.$

$R_C = \frac{V_C}{I_C} = \frac{5V}{9.3 \times 10^{-3}} = 537.6.$

DisAdvantages of fixed Bias Circuit:

* This circuit does not provide any check on the collector current which increases with the rise in temperature. ii) Thermal Stability is not provided by this Circuit. So the operating point is not maintained.

$I_C = \beta I_B + I_{CEO}$

* Since $I_C = \beta I_B$ and I_B is already fixed. I_C depends on β, which changes unit to unit and shifts the operating point.
* The stabilization of operating point is very poor in fixed bias circuit.

Advantages

* fixed bias circuit is a simple circuit which uses very few components.
* The operating point can be fixed any where in the active region of the characteristics by simply changing the value of R_B. Thus it provides maximum flexibility in design.

II. Collector to Base Bias Circuit

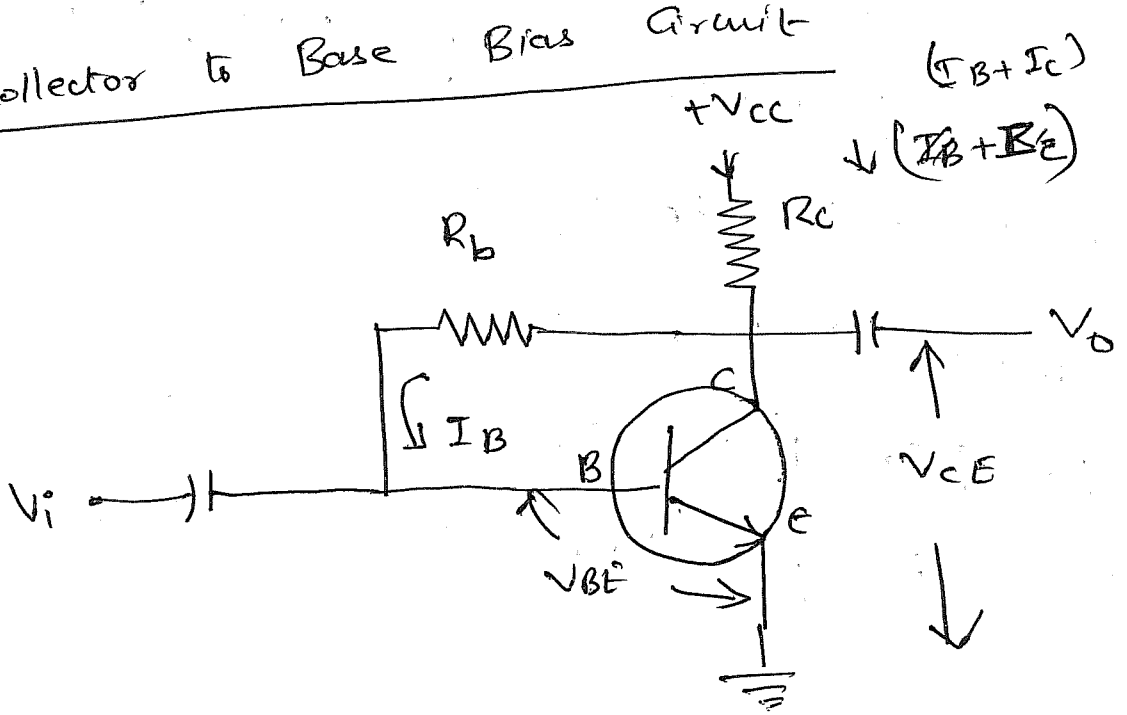


figure shows the dc bias with voltage feedback. It is also called as Collector to base bias circuit. It is an improvement over the fixed bias method. In this the biasing

resistor is connected between the collector and the base of the transistor to provide a feed back path. Thus I_B flows through R_B and $(I_C + I_B)$ flows through R_C.

Circuit Analysis:

(1) Base Circuit

Let us consider the base circuit.

Applying KVL to base circuit

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_C R_C + I_B R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_C R_C + I_B R_C + I_B R_B + V_{BE} \Rightarrow$$

$$V_{CC} = I_C R_C + (R_C + R_B) I_B + V_{BE}$$

Sub $I_C = \beta I_B$

$$V_{CC} = \beta I_B R_C + I_B (R_C + R_B) + V_{BE}.$$

$$\beta I_B R_C + I_B (R_B + R_C) = V_{CC} - V_{BE}$$

$$\beta I_B R_C + I_B R_B + I_B R_C = V_{CC} - V_{BE}$$

$$I_B R_C (\beta + 1) + I_B R_B = V_{CC} - V_{BE}.$$

$$I_B [R_C (\beta + 1) + R_B] = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C} \qquad \beta >>> 1$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}}$$

The only difference between the equation for I_B and obtained and the fixed bias I_B is only the term βR_c. Thus we can say that the feedback path results in a reflection of the resistance R_c to the input Circuit.

Collector Circuit

Applying KVL to the Collector Circuit we get

$$V_{cc} - (I_c + I_B)R_c - V_{CE} = 0$$

$$V_{CE} = V_{cc} - (I_c + I_B)R_c$$

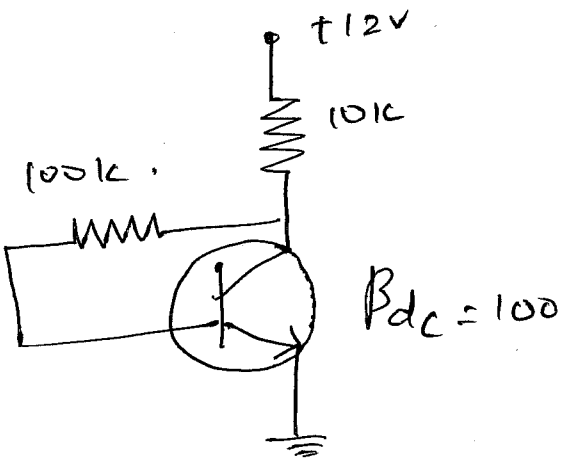
If there is a change in β due to piece to piece variation between transistor or if there is a change in ~~collector~~ current β and I_{CO} due to change in temperature then collector current I_c tends to increase. we know that,

$$I_c = \beta I_B + I_{CEO}$$

As a result voltage drop across R_c increases. As V_{cc} is constant, due to deduction in V_{CE}, I_B reduces.

In this Circuit R_B appears directly across B & C. A part of o/p is feedback to the i/p and increase in collector current decreases the base current. Thus negative feedback exists in the circuit. So the Circuit is also called as Voltage feedback bias Circuit.

Pb Calculate the Q point values I_C & V_{CE} for the Circuit Shown.



$V_{CC} = 12$

$V_B = 0.7$

$R_B = 100K$

$\beta = 100$

$R_C = 10K$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$= \frac{12 - 0.7}{100 \times 10^3 + (1+100) \times 10 \times 10^3}$$

$I_B = 10.18\ \mu A$ 10.27 μA.

$$I_C = \beta I_B = 100 \times 10.18\ \mu A = 1.018\ mA = I_C$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

$$= 12 - (10.18 \times 10^{-6} + 1.018 \times 10^{-3}) \times 10 \times 10^3$$

$$V_{CE} = 1.7182\ V$$

Pb Calculate the minimum and maximum values of I_C and V_{CE} for the Collector to base bias circuit when $h_{fe}(min) = 50$ & $h_{fe}(max) = 60$. For the Circuit $V_{CC} = 12$, $R_C = 2K$, $R_B = 150K$. Assume Silicon Transistor

Soln

(i) For h_{fe} min

$$I_B = \frac{V_{cc} - V_{BE}}{(1+\beta) R_c + R_B}$$

$$= \frac{12 - 0.7}{(1+50)\,2K + 450K}$$

$$\boxed{I_B = 44.84\,\mu A}$$

$$I_c = \beta I_B = 50 \times 44.84\,\mu A = 2.242\,mA$$

$$\boxed{I_c = 2.242\,mA}$$

$$V_{CE} = V_{cc} - (I_{B_{min}} + I_{c_{max}}) R_c$$

$$V_{CE} = 12 - (44.84\,\mu A + 2.242mA) \times 2K$$

$$V_{CE} = 7.426\,V.$$

(ii) for h_{FE} (max)

$$I_B = \frac{12 - 0.7}{(1+60)\,2K + 150K}$$

$$\boxed{I_B = 41.54\,\mu A}$$

$$I_c = \beta I_B = 60 \times 41.54\,\mu A$$

$$\boxed{I_c = 2.492\,mA}$$

$$V_{CE} = V_{cc} - (I_B + I_c) R_c$$

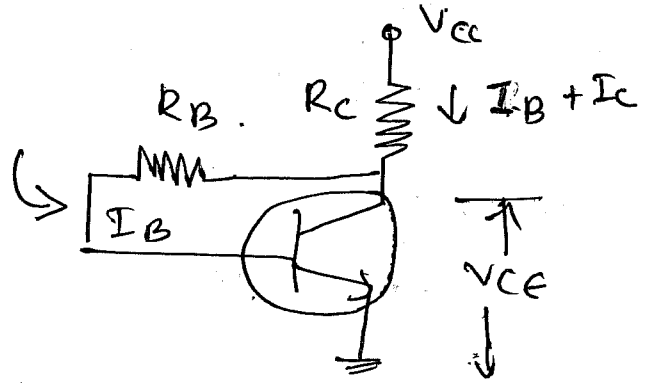
$$= V_{cc} - (I_{B_{max}} + I_{c_{max}}) R_c$$

$$V_{CE} = 12 - (41.54\,\mu A + 2.492mA) \times 2K$$

$$\boxed{V_{CE} = 6.932V}$$

DESIGN EXAMPLES

1) Design a Collector to Base bias circuit for the specified conditions. $V_{CC} = 15V$, $V_{CE} = 5V$, $I_C = 5mA$. $\beta = 100$.



Given

$I_C = 5mA$

$\beta I_B = 5mA$

$I_B = \frac{5mA}{\beta}$

$$I_B = \frac{5mA}{100} = 50\mu A$$

$$\boxed{I_B = 50\mu A}$$

We know that for a Collector to base bias ckt

$$V_{CE} = V_{CC} - (I_B + I_C)R_C \Rightarrow (I_B + I_C)R_C = V_{CC} - V_{CE}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C}$$

$$R_C = \frac{15 - 5V}{50 \times 10^{-6} + 5 \times 10^{-3}}$$

$$\boxed{R_C = 1.98\ K}$$

Applying KVL to i/p circuit, [due to feedback]

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{5 - 0.7}{50 \times 10^{-6}}$$

$$\boxed{R_B = 86\ k}$$

Ph

Design a Collector to base bias circuit to have operating point of (10V, 4mA). The circuit is supplied with 20V, and uses Silicon transistor of $h_{fe} = 250$.

Given

$V_{CEQ} = 10V$

$I_C = 4V$

$V_{CC} = 20V$

$V_{BE} = 0.7$

$h_{fe} = 250$

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta} = \frac{4mV}{250}$$

$$\boxed{I_B = 16\,\mu A}$$

W.K.T $V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$

$$V_{CC} - (I_B + I_C) R_C = 0$$

$$V_{CE} - V_{CC} - (I_B + I_C) R_C = 0$$

$$V_{CC} - V_{CE} = (I_B + I_C) R_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C}$$

$$R_C = \frac{20 - 10}{16\,\mu A + 4mA}$$

$$R_C = 2.49\,k\Omega$$

Applying KVL to i/p circuit,

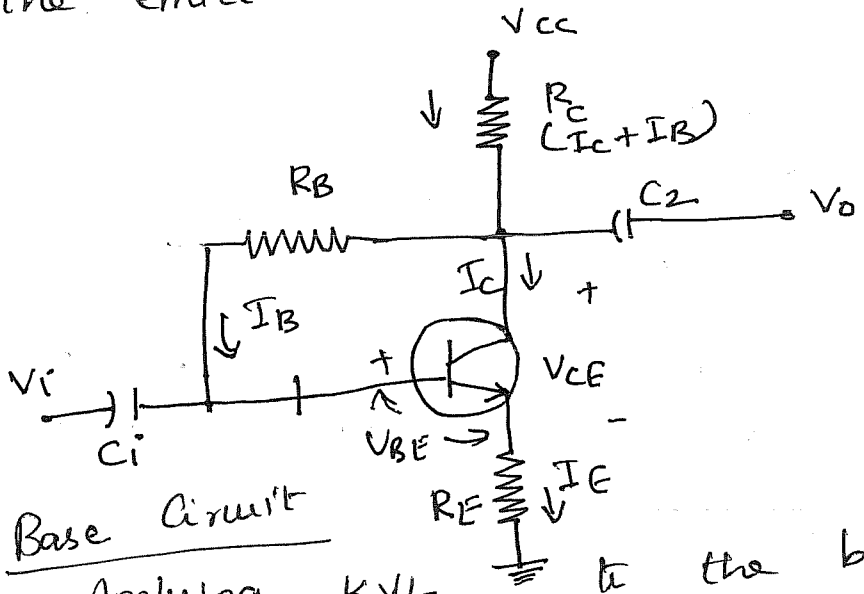
$$V_{CE} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{10 - 0.7}{16\,\mu A}$$

$$\boxed{R_B = 581.25\,k\Omega}$$

Modified Collector to Base Bias Circuit

To further improve the level of stability the emitter resistance is connected as this circuit



Base Circuit

Applying KVL to the base circuit,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - V_{BE} = (I_C + I_B)R_C + I_B R_B - I_E R_E \qquad I_E = I_C + I_B$$

$$V_{CC} - V_{BE} = I_C R_C + I_B R_C + I_B R_B + I_E R_E \qquad I_C = \beta I_B$$

$$V_{CC} - V_{BE} = \beta I_B R_C + I_B R_C + I_B R_B + I_E R_E$$

$$= (\beta+1) I_B R_C + I_B R_B + (I_C + I_B) R_E$$

$$= (\beta+1) I_B R_C + I_B R_B + (\beta I_B + I_B) R_E$$

$$V_{CC} - V_{BE} = (\beta+1) I_B R_C + I_B R_B + (\beta+1) I_B R_E$$

$$= \{(\beta+1) R_C + R_B + (\beta+1) R_E\} I_B$$

$$V_{CC} - V_{BE} = \{(\beta+1)[R_C + R_E] + R_B\} I_B$$

$$\{(\beta+1)(R_C + R_E) + R_B\} I_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C + R_E)}$$

If $\beta >> 1$,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

* The only difference between the equation of I_B and the equation for I_B obtained from fixed bias circuit is only the term $\beta(R_C + R_E)$
* Thus we can say the feedback path results the reflection of the resistance R_C back to the input circuit. The above equation can be in general,

$$I_B = \frac{V'}{R_B + \beta R'}, \quad \text{when } \beta >> 1$$

$R' = 0$ for fixed bias

$R' = R_E$ for emitter bias

$R' = R_C$ for Collector to base bias.

$R' = R_C + R_E$ for Collector to base bias with R_E.

Collector Circuit,

Applying KVL,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C - I_E R_E = 0$$

$$= V_{CC} - I_C R_C - I_B R_C - (I_C + I_B) R_E$$

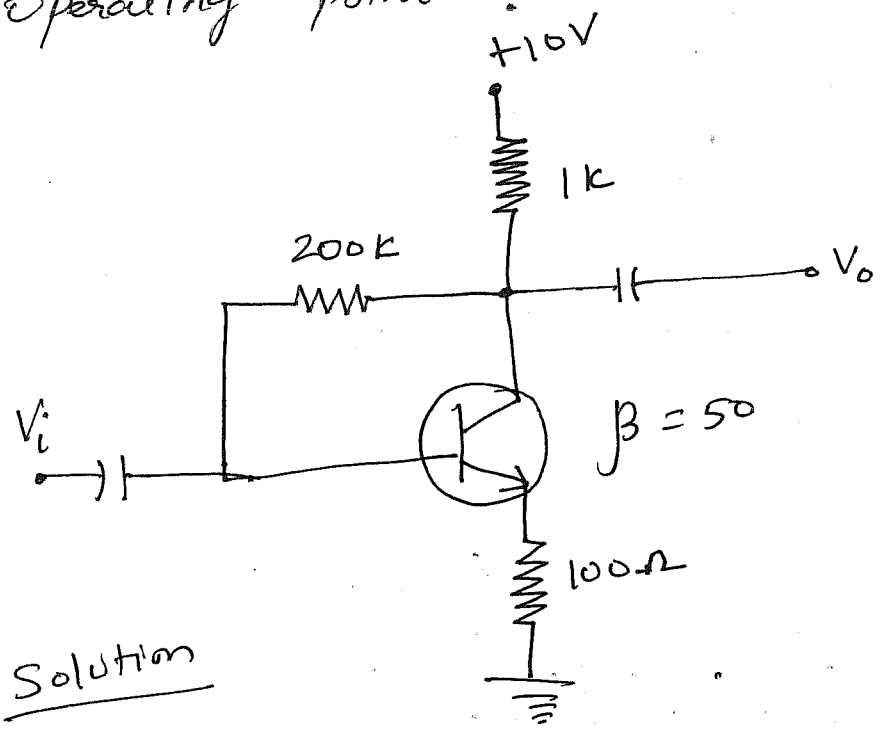
$$= V_{CC} - I_C R_C - I_B R_C - I_C R_E - I_B R_E$$

$$= V_{CC} - R_C (I_E + I_B) - (I_C + I_B) R_E$$

$$= V_{CC} - I_E R_C - I_E R_E$$

$$\boxed{V_{CE} = V_{CC} - I_E (R_C + R_E)}$$

Pb For a circuit shown in figure calculate the operating point.



Given

$V_{CC} = +10V$

$R_C = 1K$

$R_b = 200K$

$\beta = 50$

$R_e = 100\Omega$

To find

$V_{CEQ} = ?$

$I_{CQ} = ?$

Solution

$$I_{BQ} = \frac{V_{CE} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}$$

$$= \frac{10 - 0.7}{200 \times 10^3 + (1+50)(1 \times 10^3 + 100)}$$

$$\boxed{I_B = 36.31\ \mu A}$$

$$I_{CQ} = \beta I_B = 50 \times 36.31 \times 10^{-6}$$

$$\boxed{I_{CQ} = 1.8155\ mA}$$

$$I_{EQ} = I_B + I_{CQ} = 36.31 \times 10^{-6} + 1.8155 \times 10^{-3}$$

$I_{EQ} = 1.8581 mA$

$V_{CEQ} = V_{CC} - I_E (R_C + R_E)$

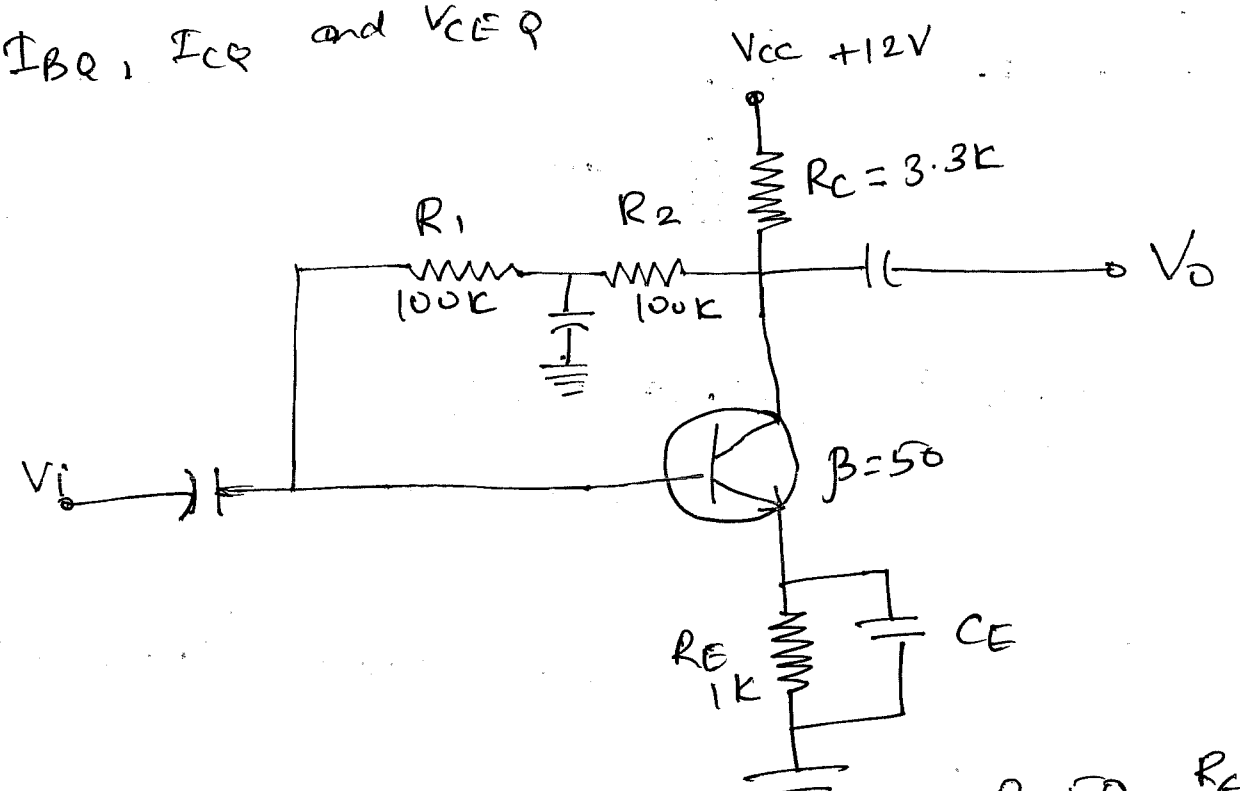
$= 10 - 1.85181 \times 10^{-3} (1 \times 10^3 + 100)$

$V_{CEQ} = 7.963 V$

The operating point is,

$V_{CEQ}, I_{CQ} = (1.8155 mA, 7.963 V)$

Ans For the circuit shown in fig determine I_{BQ}, I_{CQ} and V_{CEQ}



Given: $V_{CC} = +12V$, $R_C = 3.3K$, $\beta = 50$, $R_E = 1K$

$R_B = R_1 + R_2 = 100K + 100K$

$R_B = 200K$

To find I_{BQ}, I_{CQ}, V_{CEQ}.

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}$$

$$= \frac{12 - 0.7}{200 \times 10^3 + (1+50)(3.3 \times 10^3 + 1 \times 10^3)}$$

$$\boxed{I_{BQ} = 26.95\ \mu A}$$

$$I_{CQ} = \beta I_{BQ} = 50 \times 26.95\ \mu A = 50 \times 26.95 \times 10^{-6}$$

$$\boxed{I_{CQ} = 1.347\ mA}$$

$$I_{EQ} = I_{BQ} + I_{CQ} = 26.95 \times 10^{-6} + 1.347 \times 10^{-3}$$

$$I_{EQ} = 1.3739\ mA$$

$$V_{CEQ} = V_{CC} - I_E (R_C + R_E)$$

$$= 12 - 1.3739 \times 10^{-3} (3.3 \times 10^3 + 1 \times 10^3)$$

$$\boxed{V_{CEQ} = 6.09\ V}$$

Stability factor "S" for Collector to Base Circuit

$V_{CC} \rightarrow \frac{\partial I_C}{\partial I_B} \rightarrow S \downarrow$ $\frac{\partial I_B}{\partial I_C}$

Applying KVL to the Collector to Base bias Circuit,

$$S = (1+\beta)/1 - \beta(\partial I_B / \partial I_C)$$

$$\boxed{V_{CC} = I_C R_C + I_B (R_C + R_B) + V_{BE}} \quad \text{(A)}$$

$$V_{CC} = I_C R_C + I_B R_C + I_B R_B + V_{BE}$$

S_I = When I_{CBO} changes by ∂I_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C. These is

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B)$$

$$-\partial I_C R_C = \partial I_B (R_C + R_B)$$

$$\partial I_B = -\partial I_C \frac{R_C}{(R_C + R_b)}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B}$$

W.K.T,

$$S = \frac{1+\beta}{1-\beta(\partial I_B/\partial I_C)}$$

Sub $\frac{\partial I_B}{\partial I_C}$ in S,

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_C+R_B}\right)}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}}$$

Collector to Base bias Circuit has lesser Stability factor than fixed bias Circuit.

Stabilization with changes in β

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$\beta I_B = I_C - (1+\beta) I_{CBO}$$

$$I_B = \frac{I_C - (1+\beta) I_{CBO}}{\beta}$$

Apply KVL to base circuit we write

$V_{CC} - I_B(R_B + R_C) - I_C R_C - V_{BE} = 0$

Multiplying by (-1), $-V_{CC} + (I_B + I_C)R_C + I_B R_B + V_{BE} = 0$

$-V_{CC} + I_B R_C + I_C R_C + I_B R_B + V_{BE} = 0$

$-V_{CC} + I_B(R_C + R_B) + I_C R_C + V_{BE} = 0$

Substituting the value of I_B in the above eqn,

$$-V_{CC} + \left[\frac{I_C - (1+\beta) I_{CO}}{\beta}\right](R_C + R_B) + I_C R_C + V_{BE} = 0$$

Multiplying By β on both sides,

$-\beta V_{CC} + [I_C - (1+\beta) I_{CO}](R_C + R_B) + \beta I_C R_C + \beta V_{BE} = 0$

$-\beta V_{CC} + (R_C + R_B) I_C - (1+\beta) I_{CO}(R_C + R_B) + \beta I_C R_C + \beta V_{BE} = 0$

$$I_C[R_C + R_B + \beta R_C] = \beta V_{CC} + \frac{(1+\beta)}{\beta}(R_C + R_B) I_{CO} - \beta V_{BE}$$

$$I_C[R_C + R_B + \beta R_C] = \beta[V_{CC} - V_{BE} + I_{CO}(R_B + R_C)]$$

As $\beta >> 1$, $\beta + 1 = \beta$ in the above exp;

Also, $\beta R_C >> R_B$.

$I_C[R_C + R_B + \beta R_C]$ will be $I_C[R_C + \beta R_C]$ because $R_B + \beta R_C = \beta R_C$

$$I_C[\cdots \beta R_C] = \beta[V_{CC} - V_{BE} + I_{CO}(R_B + R_C)]$$

$$I_C = \frac{\beta[V_{CC} - V_{BE} + I_{CO}[R_B + R_C]]}{\beta R_C}$$

$$\boxed{I_C = \frac{V_{CC} - V_{BE} + I_{CO}(R_C + R_B)}{R_C}}$$

Stability factor S'

$$S' = \frac{\partial I_C}{\partial V_{BE}}\Big|_{I_{CO},\ \beta \text{ constant}}$$

from V_{CC} ↓ I_C ↓ $\frac{\partial I_C}{\partial V_{BE}} = S'$

Applying KVL to the circuit, we have

(A) $\Rightarrow V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$

$$(R_B + R_C) I_B = V_{CC} - I_C R_C - V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

w.k.t $I_C = \beta I_B$, $I_B = \frac{I_C}{\beta}$

$$\frac{I_C}{\beta} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

$$\frac{I_C}{\beta} = \frac{V_{CC} - V_{BE}}{R_C + R_B} - \frac{I_C R_C}{R_C + R_B}$$

$$\frac{I_C}{\beta} + \frac{I_C R_C}{R_C + R_B} = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$I_C \left[\frac{1}{\beta} + \frac{R_C}{R_C + R_B} \right] = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$I_C \left[\frac{R_C + R_B + \beta R_C}{\beta (R_C + R_B)} \right] = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B} \times \frac{\beta (R_C + R_B)}{(1+\beta) R_C + R_B}$$

$$\boxed{I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1+\beta) R_C}}$$

$$\therefore I_C = \frac{+\beta V_{CC}}{R_B + (1+\beta) R_C} - \frac{\beta V_{BE}}{R_B + (1+\beta) R_C}$$

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B + (1+\beta)R_C}$$

$$\boxed{S' = \frac{-\beta}{R_B + (1+\beta)R_C}}$$

Relation Between S and S''

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

$$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$$

$$S = \frac{1+\beta}{\frac{1(R_C+R_B)+\beta R_C}{R_C+R_B}} = \frac{(1+\beta)(R_C+R_B)}{R_C+R_B+\beta R_C}$$

$$S = \frac{(1+\beta)(R_C+R_B)}{(1+\beta)R_C + R_B}$$

$$\frac{S}{(1+\beta)(R_C+R_B)} = \frac{1}{R_B + (1+\beta)R_C}$$

x by $-\beta$

$$\frac{-S\beta}{(1+\beta)(R_C+R_B)} = \frac{-\beta}{R_B + (1+\beta)R_C} = S'$$

So

$$\boxed{S' = \frac{-S\beta}{(1+\beta)(R_C+R_B)}}$$

Stability factor S''

$$S'' = \frac{\partial I_C}{\partial \beta} \Big| \; I_{CO}, V_{BE} \text{ constant.}$$

For Collector to base bias circuit, applying KVL,

w.K.T, $I_C = \beta I_B$

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = (I_C + I_B) R_C + I_B R_B$$

$$V_{CC} - V_{BE} = (\beta I_B + I_B) R_C + I_B R_B$$

$$= (\beta + 1) I_B R_C + I_B R_B$$

$$V_{CC} - V_{BE} = I_B [(\beta + 1) R_C + R_B]$$

$$I_B = \frac{V_{CC} - V_{BE}}{(\beta + 1) R_C + R_B}$$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1 + \beta) R_C} \quad [\text{w.K.T}]$$

$$\frac{\partial I_C}{\partial \beta} = \frac{[R_B + (1+\beta) R_C][V_{CC} - V_{BE}] - \beta (V_{CC} - V_{BE}) R_C}{[(\beta + 1) R_C + R_B]^2}$$

$$\frac{d}{dt}\left(\frac{u}{v}\right) = \frac{v u' - u v'}{v^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{CC} - V_{BE})(\beta + 1) R_C + (V_{CC} - V_{BE}) R_B - \beta V_{CC} R_C + \beta R_C V_{BE}}{[(\beta + 1) R_C + R_B]^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{CC} - V_{BE})[(\beta + 1) R_C + R_B] - \beta R_C [V_{CC} - V_{BE}]}{[(\beta + 1) R_C + R_B]^2}$$

Taking $V_{CC} - V_{BE}$ commonly outside,

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{CC} - V_{BE})\left[(\beta+1)R_C + R_B - \beta R_C\right]}{\left[(\beta+1)(R_C + R_B)\right]^2}$$

$$= \frac{(V_{CC} - V_{BE})\left[\beta R_C + R_C + R_B - \beta R_C\right]}{\left[(\beta+1)R_C + R_B\right]^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{CC} - V_{BE})(R_C + R_B)}{\left[(\beta+1)(R_C) + R_B\right]^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{(V_{CC} - V_{BE})(R_C + R_B)}{\left[(\beta+1)R_C + R_B\right]} \times \frac{1}{\left[(\beta+1)R_C + R_B\right]}$$

we know that,

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{(\beta+1)(R_C) + R_B} \Rightarrow$$

$$\frac{I_C}{\beta} = \frac{V_{CC} - V_{BE}}{(\beta+1)R_C + R_B}$$

Sub, $\frac{I_C}{\beta}$ in $\frac{\partial I_C}{\partial \beta}$ expression

$$\frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \frac{(R_C + R_B)}{\left[(\beta+1)R_C + R_B\right]}$$

$$S'' = \frac{\partial I_C}{\partial \beta}$$

Relation between S and S''

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C(R_C + R_B)}{\beta\left[(\beta+1)R_C + R_B\right]} = \frac{I_C}{\beta} \frac{(R_C + R_B)}{\left[(\beta+1)R_C + R_B\right]}$$

w.k.t,

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)} \Rightarrow \frac{S}{1+\beta} = \frac{1}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}$$

Taking LCM & Re...

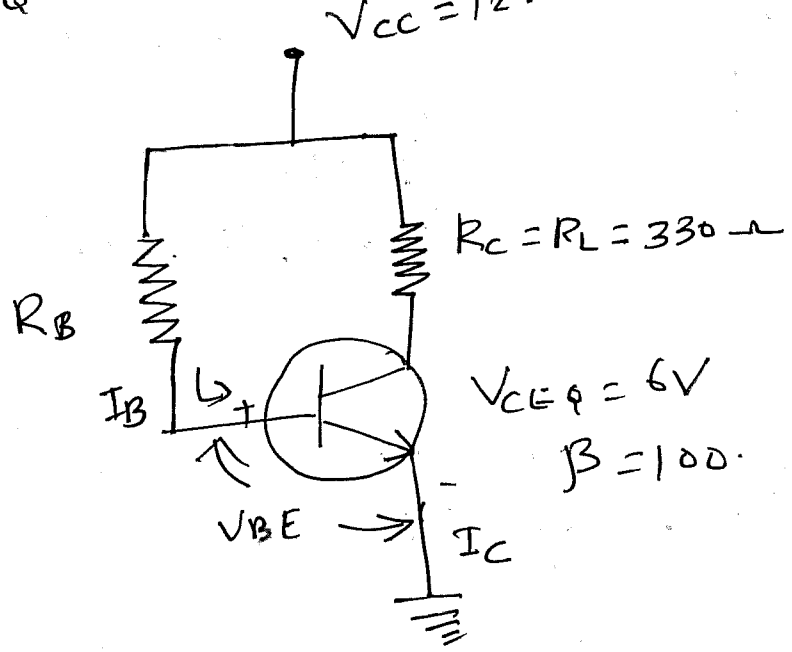
$$\Rightarrow \quad \frac{S}{1+\beta} = \frac{1}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)} = \frac{(R_C+R_B)}{R_B+(1+\beta)R_C}$$

$$S'' = \frac{I_C (R_B+R_C)}{\beta(\beta+1)(R_E)+R_B}$$

$$S'' = \frac{I_C}{\beta} \cdot \frac{S}{1+\beta}$$

$$\boxed{S'' = \frac{I_C}{\beta}\left(\frac{S}{(1+\beta)}\right)}$$

Pb Determine the bias resistor R_B for the fixed bias and Collector to base bias and Compare the stability factor S for both of them. Given $V_{CC} = 12V$, $R_L = 330\,\Omega$. $I_B = 0.3mA$, $\beta = 100$, $V_{CEQ} = 6V$.



To find

$R_B = ?$

$S = ?$ for both fixed and collector & base bias circuit.

Fixed Bias Circuit

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{0.3 \times 10^{-3}} = 37.67\ k\Omega$$

$$S = 1 + \beta \Rightarrow 1 + 100$$

$$\boxed{S = 101}$$

Collector to Base bias Circuit

Applying KVL,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$12 - [(0.3 \times 10^{-3}) + (0.3 \times 10^{-3})] \times 100 \times 330 - 0.3 \times 10^{-3} \times R_B - 0.7 = 0$$

$$R_B = \frac{12 - 9.999 - 0.7}{0.3 \times 10^{-3}} = \frac{1.301}{0.1 \times 10^{-3}}$$

$$\boxed{R_B = 4.3367\ k\Omega}$$

$$\text{Stability factor} = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}$$

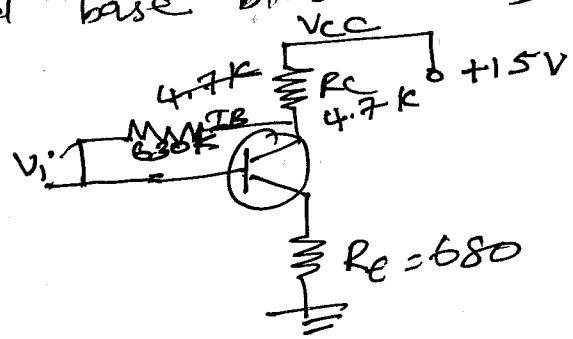
$$S = \frac{1+100}{1+100\left(\frac{330}{300 + 4336.7}\right)}$$

$$\boxed{S = 12.4428}$$

Pb Locate the operating point of the circuit shown in fig. $V_{CC} = 15V$, $h_{fe} = 200$

Soln

The base current for a Base bias circuit with emitter (modified base bias circuit) is



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}$$

$$= \frac{15 - 0.7}{630 \times 10^3 + (1+200)(4.7 \times 10^3 + 680)}$$

$$\boxed{I_B = 8.356\ \mu A}$$

$$I_{CQ} = \beta I_{BQ} = 200 \times 8.356 \times 10^{-6}$$

$$I_{CQ} = 1.6712\ mA$$

Apply KVL to collector,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_E R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_E (R_C + R_E)$$

$$I_{EQ} = I_{CQ} + I_{BQ}$$

$$= 1.66 \times 10^{-3} + 8.356 \times 10^{-6}$$

$$I_{EQ} = 1.68\ mA$$

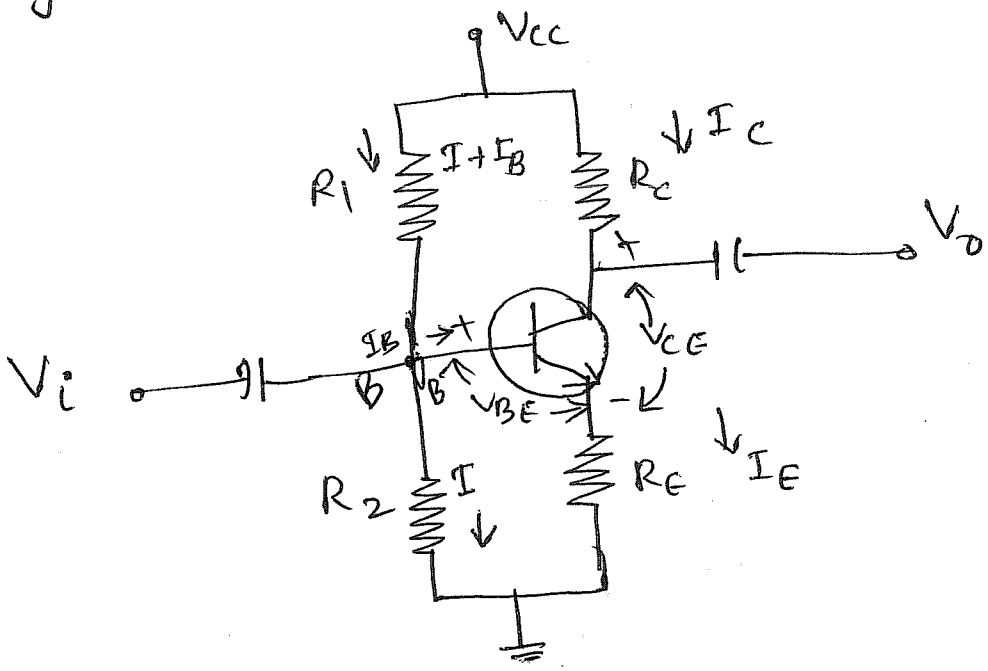
$$V_{CEQ} = V_{CC} - I_E (R_C + R_E) = 15 - 1.68 \times 10^{-3} (4.7 \times 10^3 + 680)$$

$V_{CEQ} = 5.96\ V$

Operating Point = (5.96 V, 1.67 mA)
(V_{CEQ}, I_{CQ})

VOLTAGE DIVIDER BIAS CIRCUIT (OR) SELF BIAS CIRCUIT.

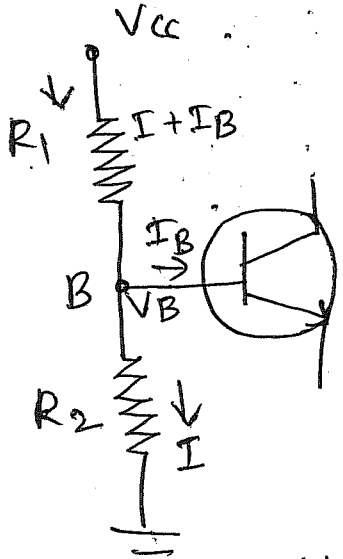
Voltage divider Bias / Self Bias Circuit



Circuit Analysis

Base Circuit

Let us Consider the base circuit as shown in the fig.



Voltage across R_2 is the base voltage V_B.
Applying the Voltage divider theorem to find V_B,

$$V_B = \frac{R_2 \times I}{R_1 (I + I_B) + R_2 (I)} \times V_{CC}$$

$I \gg I_B$ Hence I_B can be neglected.

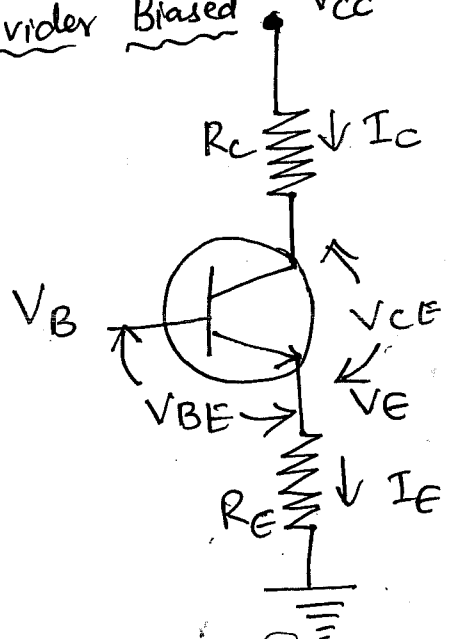
$$V_B = \frac{R_2 \times I}{R_1 I + R_2 I} \times V_{CC}$$

$$= \frac{R_2 \cancel{I}}{(R_1 + R_2)\cancel{I}} \times V_{CC}$$

$$\boxed{V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}.}$$

Collector Circuit

Consider the collector circuit as shown in the fig. Divider Biased



Voltage across R_E is V_E

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0 \quad \text{---(1)}$$

$$V_B - V_{BE} - V_E = 0 \quad \text{---(2)}$$

Voltage across R_E, V_E can be obtained by

$$V_E = V_B - V_{BE}$$

$$V_E = I_E R_E$$

$$V_E = I_E R_E = V_B - V_{BE}$$

$$I_E R_E = V_B - V_{BE}$$

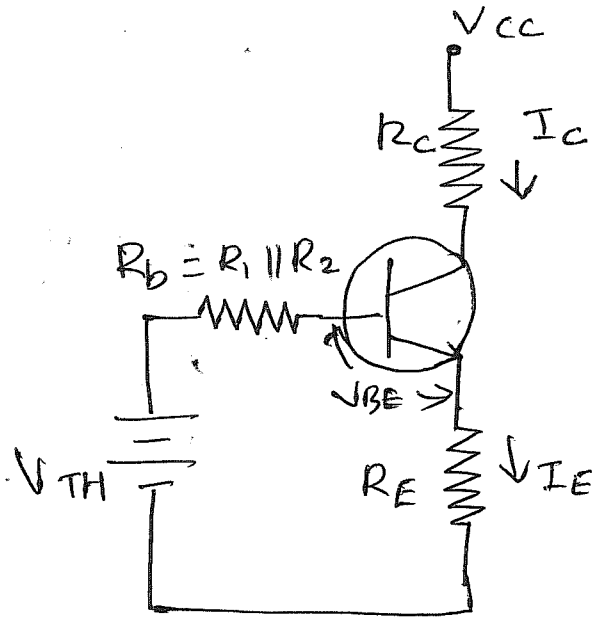
$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E}$$

Simplified Circuit of Voltage Divider Bias



$$V_{TH} - I_B R_B - V_{BE} - I_E R_E = 0$$

Figure shows simplified circuit of voltage divider bias. Here R_1 and R_2 are replaced by R_B and R_B is the parallel combination of R_1 & R_2. V_{TH} is the Thevenin's voltage.

$$R_B = \frac{R_1 + R_2}{R_1 + R_2}$$

Applying KVL to the base circuit,

$$V_{TH} - I_B R_B + V_{BE} + I_E R_E = 0$$

$$V_{TH} = I_B R_B + V_{BE} + I_E R_E$$

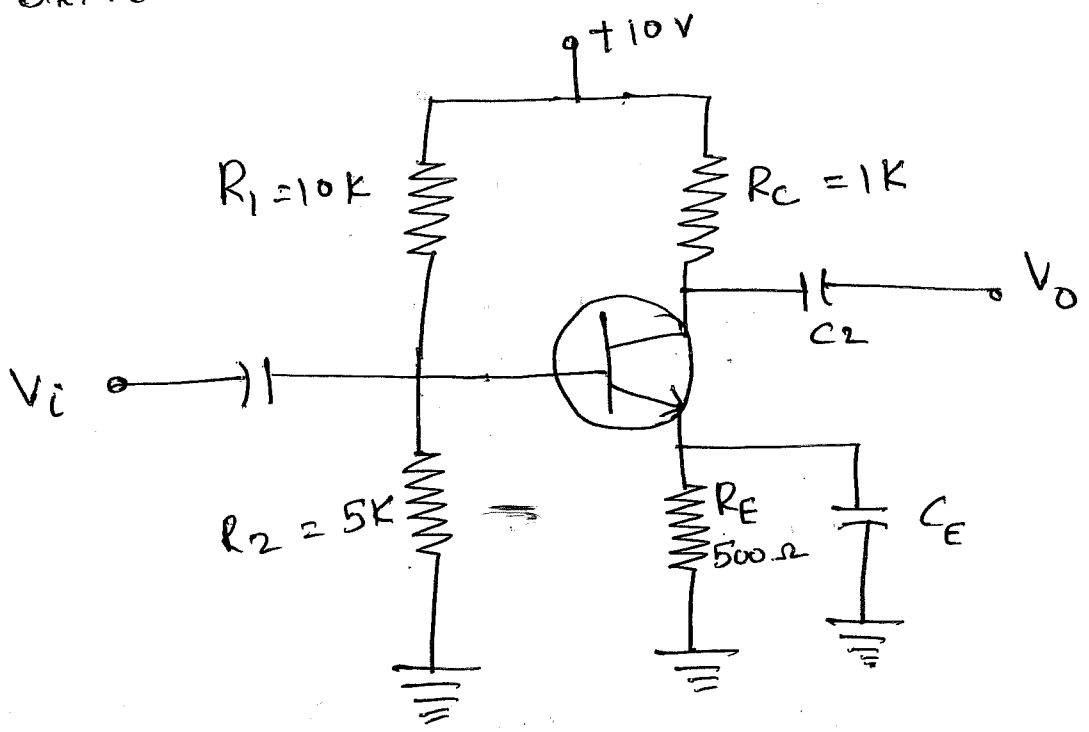
$$V_{TH} = V_{BE} + I_B R_B + (I_C + I_B) R_E$$

$$= V_{BE} + I_B R_B + I_C R_E + I_B R_E$$

$$V_{TH} = V_{BE} + I_B (R_B + R_E) + I_C R_E$$

$$V_{BE} = V_{TH} - (R_B + R_E) I_B - I_C R_E$$

Pb For the circuit shown in fig $\beta = 100$ for the silicon transistor. Calculate V_{CE} and I_C.



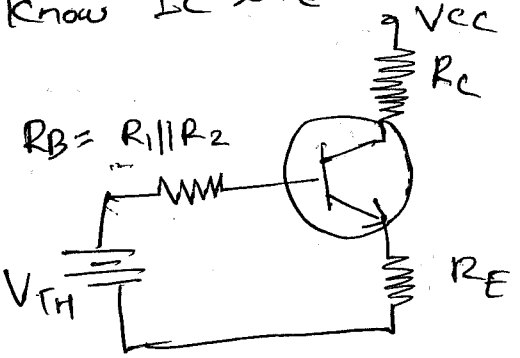
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Given: $R_1 = 10K$, $R_2 = 5K$, $R_C = 1K$, $R_E = 500\Omega$

To find V_{CE} we have to know I_C & I_E values.

$I_C = \beta I_B$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$$



Applying KVL on the base circuit,

$V_{TH} - I_B R_B - V_{BE} - I_E R_E = 0$

$V_{TH} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$

$V_{TH} - I_B R_B - V_{BE} - \beta I_B R_E - I_B R_E = 0$

$$V_{TH} - I_B R_B - V_{BE} + \beta I_B R_E + I_B R_E = 0$$

$$V_{TH} - V_{BE} = I_B R_B + \beta I_B R_E + I_B R_E$$

$$= I_B R_B + I_B R_E (\beta + 1)$$

$$V_{TH} - V_{BE} = I_B [R_B + (\beta + 1) R_E]$$

$$I_B [R_B + (\beta + 1) R_E] = V_{TH} - V_{BE}$$

$$\boxed{I_B = \frac{V_{TH} - V_{BE}}{R_B + (\beta + 1) R_E}}$$

$$R_B = R_1 \| R_2 = 10K \| 15K = \frac{R_1 R_2}{R_1 + R_2} = \frac{10K \times 5K}{10K + 5K}$$

$$\boxed{R_B = 3.33\,K}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$V_{TH} = \frac{5 \times 10^3}{10K + 5K} \times 10V$$

$$\boxed{V_{TH} = 3.33V}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1 + \beta) R_E} = \frac{3.33 - 0.7}{3.33 + (1 + 100) 500}$$

$$\boxed{I_B = 48.86\,\mu A}$$

$$I_C = \beta I_B = 100 \times 48.86\,\mu A = 4.866\,mA$$

$$I_C = 4.886\,mA.$$

$I_E = I_C + I_B$

$= 4.886\,mA + 48.86\,\mu A$

$I_E = 4.886 \times 10^{-3} + 48.86 \times 10^{-6}$

$I_E = 4.935\,mA.$

Applying KVL to Collector Circuit,

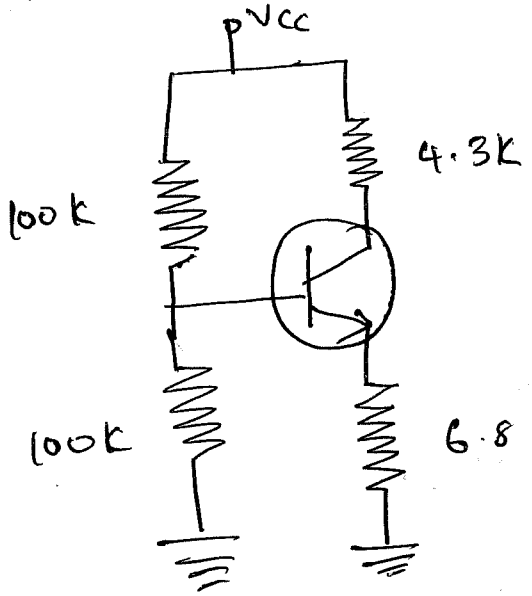
$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$V_{CE} = 10 - 4.886 \times 1K - 4.935 \times 10^{-3} \times 500$

$\boxed{V_{CE} = 2.6465\,V}$

Pb For the transistor circuit shown in figure find @ point, $V_{CC} = 15\,V$ and $\beta = 100$, $V_{BE} = 0.7\,V$



Given

$R_1 = 100K$, $R_2 = 100K$, $R_C = 4.3K$, $R_E = 6.8K.$

$V_{CC} = 15V$, $\beta = 100$, $V_{BE} = 0.7$

To find, $V_{CE} = ?$.

The Q point. $I_C = ?$.

Q point is (V_{CEQ}, I_{CQ})

$$I_C = \beta I_B$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$V_{TH} = \frac{100 \times 10^3}{100 \times 10^3 + 100 \times 10^3} \times 15$$

$$\boxed{V_{TH} = 7.5\ V}$$

$$R_B = \frac{R_2}{R_1 + R_2} = \frac{100}{100+100} = \frac{100}{200} = \frac{1}{2} = 0.5.$$

$$\boxed{R_B = 50K}$$

$$I_B = \frac{7.5 - 0.7}{50K + (1+100)\ 6.8 \times 10^3}$$

$$\boxed{I_B = 9.23\ \mu A}$$

$$I_C = \beta I_B$$

$$= 100 \times 9.23\ \mu A$$

$$\boxed{I_C = 0.932\ mA}$$

Applying KVL to the Collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$= 15 - 0.923\,mA \times 4.3K - 0.932 \times 6.8$

$V_{CE} = 4.6935\,V$

∴ The Q Point,

$I_{CQ}, V_{CEQ} = (0.923, 4.6935)$

Pb Calculate the minimum and maximum Values of I_C and V_{CE} for the voltage divider Bias circuit when $h_{fe(min)} = 50$ and $h_{fe(max)} = 6$ for circuit $V_{CC} = 12V$, $R_1 = 10K$, $R_2 = 2K$, $R_E = 470\,\Omega$ and $R_C = 2K$. Asume Silicon transistor.

Given

$h_{fe(min)} = 50$, $h_{fe(max)} = 60$, $V_{CC} = 12V$, $R_1 = 10K$

$R_2 = 2K$, $R_E = 470\,\Omega$, $R_C = 2K$

To find

$I_{C\,min} = ?$, $V_{CE\,min} = ?$,

$I_{C\,max} = ?$, $V_{CE\,max} = ?$.

Solution

$$I_{C\,min} = \beta_{min} I_B$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$= \frac{2 \times 10^3}{10 \times 10^3 + 2 \times 10^3} \times 12.$$

$V_{TH} = 2V$

$R_B = R_1 \| R_2 = 10K \| 2K = \frac{10K \times 2K}{10K + 2K}$

$R_B = 1.67\ K\Omega$.

i) $h_{fe\,min}$

$$I_B = \frac{2 - 0.7}{1.67 \times 10^3 + (1+50)\,470}$$

$I_B = 50.7\,\mu A$

i) For $h_{fe\,(min)}$

$I_{C_{min}} = \beta I_B = h_{fe\,min} I_B$

$I_{C\,min} = 50 \times 50.7\,\mu A$

$I_{C\,min} = 2.535\ mA$

Apply KVL for Collector Circuit,

$V_{CC} - V_{CE} - I_C R_C - I_E R_E = 0$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$V_{CE} = 12 - 2.535 \times 2k - I_E \times 470\ \Omega$

To find I_E,

$I_E = I_C + I_B = I_{C\,min} + I_B = 2.535 + 50.7\,\mu A$

$I_E = 2.5857\ mA$

$V_{CE} = 12 - 2.535 \times 2K - 2.5857 \times 470$

$V_{CE_{min}} = 5.715\ V$

(11) For $h_{fe}(max)$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (+\beta_{max}) \cdot R_E}$$

$$I_B = \frac{2 - 0.7}{1.67 \times 10^3 + (1+60) \times 470}$$

$$\boxed{I_B = 42.847\ \mu A}$$

$$I_{C_{max}} = \beta_{max} I_{B_{max}}$$

$$= 60 \times 42.847\ \mu A$$

$$\boxed{I_{C_{max}} = 2.57\ mA}$$

$$I_E = I_C + I_B = 2.57\ mA + 42.847\ \mu A.$$

$$\boxed{I_E = 2.6137\ mA}$$

$$V_{CE_{max}} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CEmax} = 12 - 2.57\ mA \times 2K - 2.6137\ mA \times 400\Omega$$

$$\boxed{V_{CE_{max}} = 5.632V}$$

Ans

$h_{fe}(mid)$

$I_C = 2.535\ mA$

$V_{CE} = 5.715\ V$

$h_{fe}(max)$

$I_C = 2.57\ mA$

$V_{CE} = 5.632V.$

Pb Analyze a BJT with voltage divider bias circuit, and determine the change in Q point with a variation in β when the circuit contains an emitter resistor. Let the biasing resistors be, $R_{B1} = 56K$, $R_{B2} = 12.2K\Omega$, $R_C = 2K$, $R_E = 0.4K$, $V_{CC} = 10V$, $V_{BE(ON)} = 0.7V$, $\beta = 100$.

Given data

$R_{B1} = 56K$, $R_{B2} = 12.2K$, $R_C = 2K$, $R_E = 0.4K$, $V_{CC} = 10V$, $V_{BE(ON)} = 0.7V$, $\beta = 100$.

To find

V_{CEQ}, I_{CQ} for different β values.

Solution

$$I_{CQ} = \beta I_{BQ}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \frac{12.2}{56+12.2} \times 10$$

$$\boxed{V_{TH} = 1.79\,V}$$

$$R_{TH} = R_1 \| R_2 = 56 \| 12.2 = \frac{56 \times 12.2}{56 + 12.2}$$

$$\boxed{R_{TH} = 10\,K\Omega}$$

$$I_B = \frac{1.79 - 0.7}{10K + (1+100) \times 0.4K}$$

$$\boxed{I_B = 21.6\,\mu A}$$

$I_{EQ} = I_{BQ} + I_{CQ} = 100 \times 21.6\ \mu A$

$I_{EQ} = 2.18\ mA$

$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$

$V_{CEQ} = 10 - (2.16\ mA)(2\ k) - 2.18\ mA \times 0.4\ k$

$\boxed{V_{CEQ} = 4.81\ V}$

(i) For $\beta = 50$,

$$I_{BQ} = \frac{1.79 - 0.7}{10 + (1+50)0.4} = 35.9\ \mu A$$

$\boxed{I_{BQ} = 35.9\ \mu A}$

$I_{CQ} = 50 \times 35.9\ \mu A = 1.8\ mA$

$\boxed{I_{CQ} = 1.8\ mA}$

$I_{EQ} = I_{CQ} + I_{BQ} = 35.9\ \mu A + 1.8\ mA$

$\boxed{I_{EQ} = 1.8359\ mA}$

$V_{CEQ} = 10 - (1.8)(2) - (1.8359)0.4)$

$\boxed{V_{CEQ} = 5.67\ V}$

(ii) For $\beta = 150$,

$$I_{BQ} = \frac{1.79 - 0.7}{10 + (1+150) \times 0.4}$$

$\boxed{I_{BQ} = 15.5\ \mu A}$

$I_{CQ} = \beta I_B$

$I_{CQ} = 150 \times 15.5\ \mu A$

$\boxed{I_{CQ} = 2.325\ mA}$

$I_{EQ} = I_{BQ} + I_{CQ}$

$= 15.5\ \mu A + 2.325\ mA$

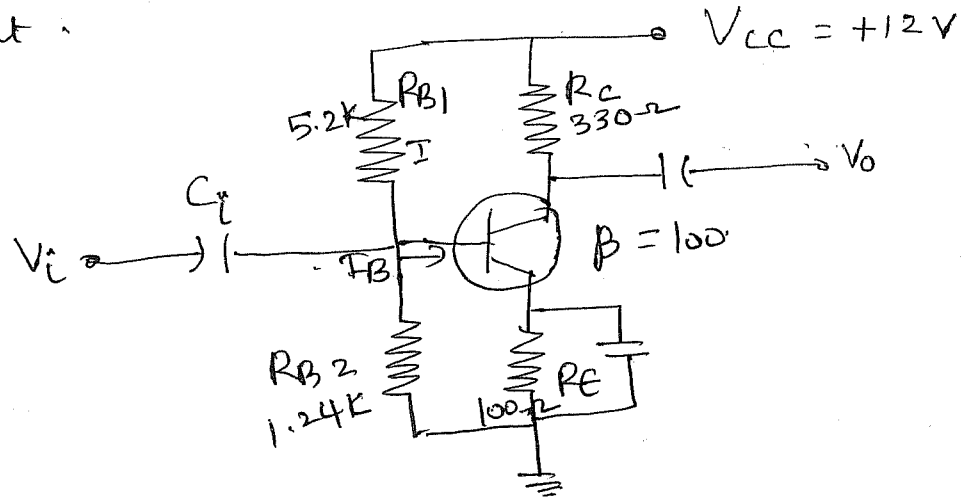
$\boxed{I_{EQ} = 2.34\ mA}$

$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E$

$= 10 - (2.325)(2k) - 2.34mA \times 0.4\ k$

$\boxed{V_{CEQ} = 4.414\ V}$

pb Draw the dc load line for the following transistor configuration. Obtain the quiescent point.



Given

$R_{B1} = 5.2k$, $R_{B2} = 1.24k$, $R_E = 100\Omega$, $R_C = 330\Omega$

$V_{CC} = +12V$, $\beta = 100$.

To find, (V_{CEQ}, I_{CQ}) To draw the Operating Point on load line.

$I_C = \beta I_B \Rightarrow I_{CQ} = \beta I_{BQ}$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$R_B = R_{TH} = \frac{R_1 \cdot R_2}{R_1 + R_2} = R_{B1} \parallel R_{B2} = \frac{R_{B2} \times R_{B1}}{R_{B1} + R_{B2}} = \frac{5.2K \times 1.24}{5.2k + 1.24k}$$

$$V_{TH} = \frac{V_{CC} \; R_{B2}}{R_{B1} + R_{B2}} = \frac{12 \times 1.24K}{5.2K + 1.24k}$$

$$\boxed{V_{TH} = 2.31\,V}$$

$$R_B = R_{TH} = \frac{5.2k \times 1.24}{5.2K + 1.24K} = 1K$$

$$\boxed{R_B = R_{TH} = 1K}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{2.31 - 0.7}{1K + (1+100)\,100\Omega}$$

$$\boxed{I_B = 145\,\mu A}$$

$$I_C = \beta I_B = 100 \times 145\,\mu A$$

$$\boxed{I_C = 14.5\,mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 12 - (14.5\,mA \times 330) - (101 \times 145\,\mu A \times 10\Omega)$$

$$= 12 - 4.785 - 1.4645$$

$$\boxed{V_{CEQ} = 5.705\,V}$$

To draw the DC load line

Point A,

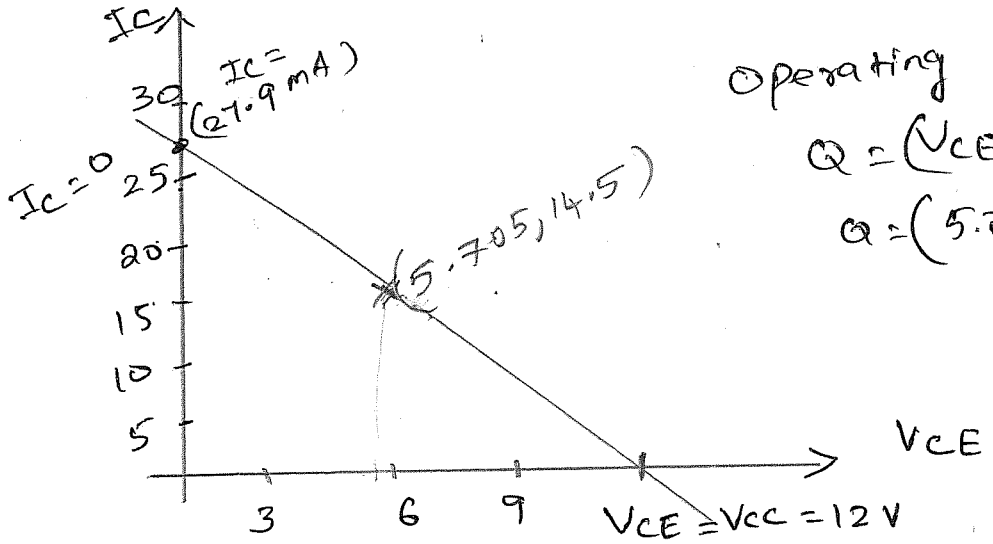
$V_{CE} = V_{CC}$ = A Point.

$V_{CE} = 12V$ = A Point.

Point B,

$$I_{CEQ} = \frac{V_{CC}}{R_C + R_E} = \frac{12}{330\Omega + 100\Omega} = 27.9mA.$$

When $I_C = 0$ and $V_{CE} = V_{CC}$.



Operating point (Q)

$Q = (V_{CE,Q}, I_{CQ})$

$Q = (5.705V, 14.5mA)$

Stability factor for Voltage Divider Bias Circuit.

(i) $$S = (1+\beta)\frac{1 + R_B/R_E}{(1+\beta) + R_B/R_E}$$

(ii) $$S' = \frac{-\beta}{R_B + (1+\beta)R_E}$$

(iii) $$S'' = \frac{I_{C_1} S_2}{\beta_1 (1+\beta_2)}$$

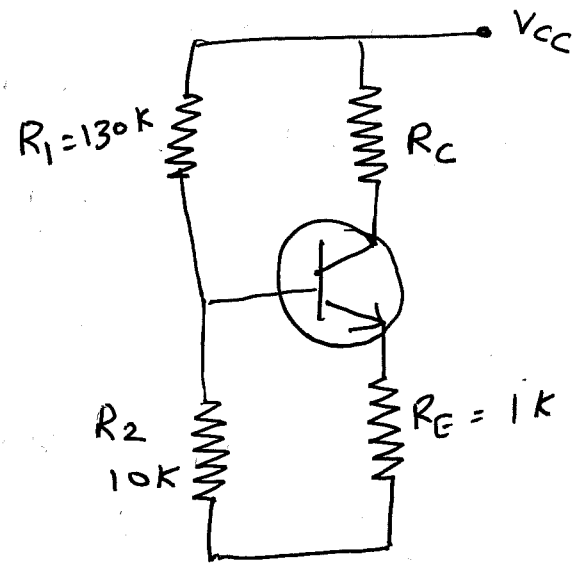
where $S_2 = \dfrac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta)R_E}$

Hint

Minimizing 'S' also minimizes S''. This means that the ratio R_B / R_E must be small to have better stability.

Pb A self bias circuit has $R_E = 1k$, $R_1 = 130k$, $R_2 = 10k$. If V_{cc} and R_c are adjusted to give $I_C = 1mA$, at $10^\circ C$, Calculate the variation in I_C over temperature range of $10^\circ C$, to $100^\circ C$. The transistor used has parameters given below

Parameters	$10^\circ C$	$100^\circ C$
I_{CO} (μA)	0.01	1.2
V_{BE} (Volts)	0.74	0.54
β	60	140



Solution:

For the self bias (Voltage divider bias) circuit as shown in fig at 10°c

Given $I_C = 1mA$, I_{CO} @ 10°C = 0.01 μA, I_{CO} @ 100°C = 1.2μA

$\Delta I_{CO} = I_{CO}$ @ 10°C to I_{CO} @ 100°C

$= 0.01 \sim 1.2$

$= 1.2 - 0.01$

$$\boxed{\Delta I_{CO} = 1.19\ \mu A}$$

$R_E = 1K$, $R_1 = 130K$, $R_2 = 10K$

$\partial V_{BE} = V_{BE2} - V_{BE1}$

$= 0.54 - 0.74$

$$\boxed{\partial V_{BE} = 0.2V}$$

$$\boxed{\partial\beta = \beta_2 - \beta_1}$$

$= 140 - 60$

$$\boxed{\partial\beta = 80}$$

$R_B = R_1 \,||\, R_2$

$R_B = 130K \,||\, 10K$

$R_B = \frac{130 \times 10\ K}{130 + 10\ K}$

$$\boxed{R_B = 9.29\ K}$$

To find

Variation in I_C ie ∂I_C w.k.t, for a self bias circuit or voltage divider bias circuit

$$\boxed{\partial I_C = S\partial I_{CO} + S'\partial V_{BE} + S''\partial\beta}$$

S, S' & S'' should be calculated.

The value of 'S' for self bias is

$$S = \frac{(1+\beta)\left(1+\frac{R_B}{R_E}\right)}{1+\beta+\frac{R_B}{R_E}}$$

$$S = \frac{(1+60)\left(1+\frac{9.29K}{1K}\right)}{1+60+\frac{9.29K}{1K}}$$

$$S = \frac{627.69}{70.29}$$

$$\boxed{S = 8.93}$$

$$S' = \frac{-\beta \frac{I}{R_E}}{1+\beta+\frac{R_B}{R_E}}$$

$$S' = \frac{-60/1K}{1+60+\frac{9.29K}{1K}} = -0.85\times10^{-3}$$

$$\boxed{S' = -0.85\times10^{-3}}$$

$$S'' = \frac{I_{C1}\, S_2}{\beta}$$

$S_2 = S$ when $\beta = \beta_2$

$$S_2 = \frac{(1+\beta_2)\left(1+\frac{R_B}{R_E}\right)}{1+\beta_2+R_B/R_E} = \frac{(1+140)\left(1+\frac{9.29K}{1K}\right)}{1+140+\left(\frac{9.29K}{1K}\right)}$$

$$S_2 = 9.65$$

$$S'' = \frac{I_{C1} S_2}{\beta} \qquad I_C = I_{C1} = 1mA$$

$$S'' = \frac{1\times10^{-3} \times 9.65}{60\,(140+1)} = \frac{1\times10^{-3}\times 9.65}{60\times141}$$

$$S'' = 1.140\times10^{-6}$$

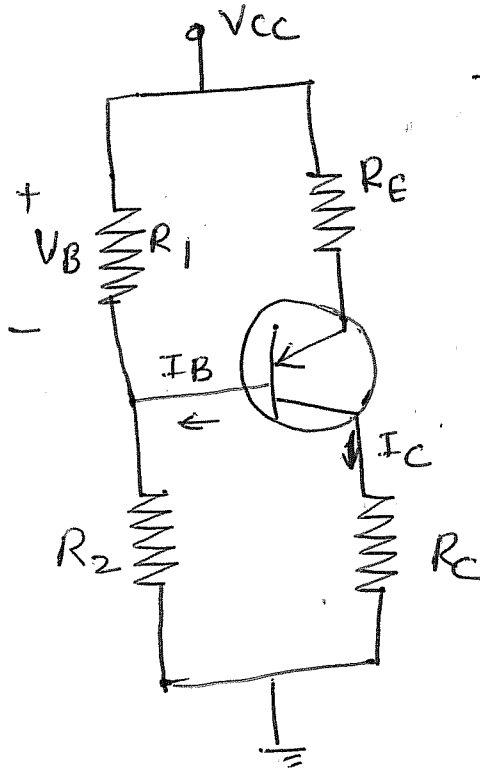
$$\partial I_C = S\partial I_{CO} + S'\partial V_{BE} + S''\partial\beta$$

$$\partial I_C = 8.93\times(1.19\,\mu A) + (-0.85\times10^{-3}\times -0.2\,V) + 1.140\times10^{-6}\times 80$$

$$\partial I_C = 10.63\,\mu A + 0.17\,mA + 92\,\mu A$$

$$\boxed{\partial I_C = 272.63\,\mu A}$$

VOLTAGE DIVIDER (SELF BIAS) Using PNP Transistor



$V_E = I_E R_E$

V_{CE}

$V_C = I_C R_C$

Only the position of R_E & R_C resistors are changed.

$$R_B = \frac{R_1 R_2}{R_1 + R_2}, \qquad I_E = \frac{V_B - V_{BE}}{R_E}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Design Examples [Voltage Divider Bias]

Ex For the voltage divider bias $V_{CC} = 5V$, $\beta = 100$, $R_C = 1.2k$, obtain the values of R_E, R_1 and R_2 such that the circuit is considered bias stable at $V_{CEQ} = 3V$.

$V_{CC} = 5V$
$\beta = 100$
$R_C = 1.2k$

Soln

Step: 1 choose R_E

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} = \frac{5-3}{1.2K + R_E}$$

When $I_C = I_E$, choose a standard value $0.68\,K$ for R_E,

$$I_C = \frac{5-3}{1.2K + 0.68} = 1.064\,mA.$$

$$\boxed{I_C = 1.064\ mA}$$

The voltage drop across R_E is V_E

$$V_E = I_E \times R_E$$

$$V_E = I_C \times R_E \quad [I_E = I_C]$$

$$V_E = 1.064 \times 0.68$$

$$\boxed{V_E = 0.7235.V}$$

Step: 2

To find I_B,

$$I_B = \frac{I_C}{\beta} = \frac{1.064 \times 10^{-3}}{100} = 10.64\,\mu A$$

$$\boxed{I_B = 10.64\ \mu A}$$

Step : 3

To find R_B

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$$

For a stable circuit,

$$R_B = 0.1 (1+\beta) R_E$$

$$R_B = 0.1 (1 + 100) \times 680$$

$$\boxed{R_B = 6.868 \text{ k}}$$

$\beta = 100$

$R_E = 0.68\text{K}$ as per standard value.

$R_E = 0.68\text{k}$

$= 0.68 \times \frac{3}{10}$

$R_E = 680$

Step : 4 To find V_{TH}

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$V_{TH} - V_{BE} = I_B (R_B + (1+\beta) R_E)$$

$$V_{TH} = V_{BE} + I_B (R_B + (1+\beta) R_E)$$

$$V_{TH} = 0.7 + 10.64\ \mu A \left(6.868\text{K} + (1+100) 680\right)$$

$$V_{TH} = 0.7 + 10.64 \times 10^{-6} \left[6.868 \times 10^3 + (101)(680)\right]$$

$$\boxed{V_{TH} = 1.5\text{ V}}$$

Step : 5 To find R_1 & R_2

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$\frac{R_2}{R_1 + R_2} \cdot V_{CC} = V_{TH}$$

$$\frac{R_2}{R_1+R_2} = \frac{V_{TH}}{V_{CC}} = \frac{1.5}{5} = 0.3$$

$$\frac{R_2}{R_1+R_2} = 0.3$$

$$R_B = \frac{R_1 R_2}{R_1+R_2} = R_1 \cdot \frac{R_2}{R_1+R_2} = R_1 \times 0.3$$

$$R_B = 0.3 R_1$$

$$0.3 \times R_1 = R_B$$

$$R_1 = \frac{R_B}{0.3}$$

$R_B = 6.868\ K$

$$R_1 = \frac{6.868\ K}{0.3}$$

$\boxed{R_1 = 22.9\ K}$ Standard Value.

$$R_2 = \frac{1}{\frac{1}{R_B} - \frac{1}{R_1}}$$ [Standard formula]

$$= \frac{1}{\frac{1}{6.86K} - \frac{1}{22.9K.}}$$

$$R_2 = \frac{1}{0.147\ K - 0.0436\ K}$$

$$= \frac{1}{0.1034} = 9.7$$

$\boxed{R = 9.7\ K\Omega}$ Standard Value.

Design a voltage divider bias circuit for the specified conditions. $V_{CC} = 12V$, $V_{CE} = 6V$, $I_C = 1mA$, $S = 20$, $\beta = 100$, $V_E = 1V$

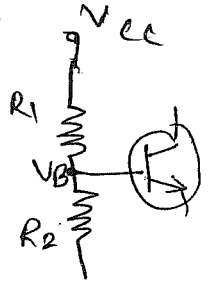
Soln

Step: 1

Obtain I_B an I_E

$$I_B = \frac{I_C}{\beta}$$

Voltage Divider Bias (Self Bias) BJT.



1. $V_B = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$

2. $V_{TH} = V_B$, $R_B = R_1 \| R_2$.

3. $I_E = \frac{V_B - V_{BE}}{R_E}$ &

4. $V_{BE} = V_B - V_E$

5. $V_{CE} = V_C - V_E$

6. $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

7. $R_B = \frac{R_1 R_2}{R_1 + R_2}$

8. $I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$

9. $I_C = \beta I_B$

10. $I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$ when I_E is equal to I_C.

11. $S = (1+\beta) \frac{1 + R_B/R_E}{(1+\beta) + R_B/R_E}$

12. $S' = \frac{-\beta}{R_B + (1+\beta) R_E}$

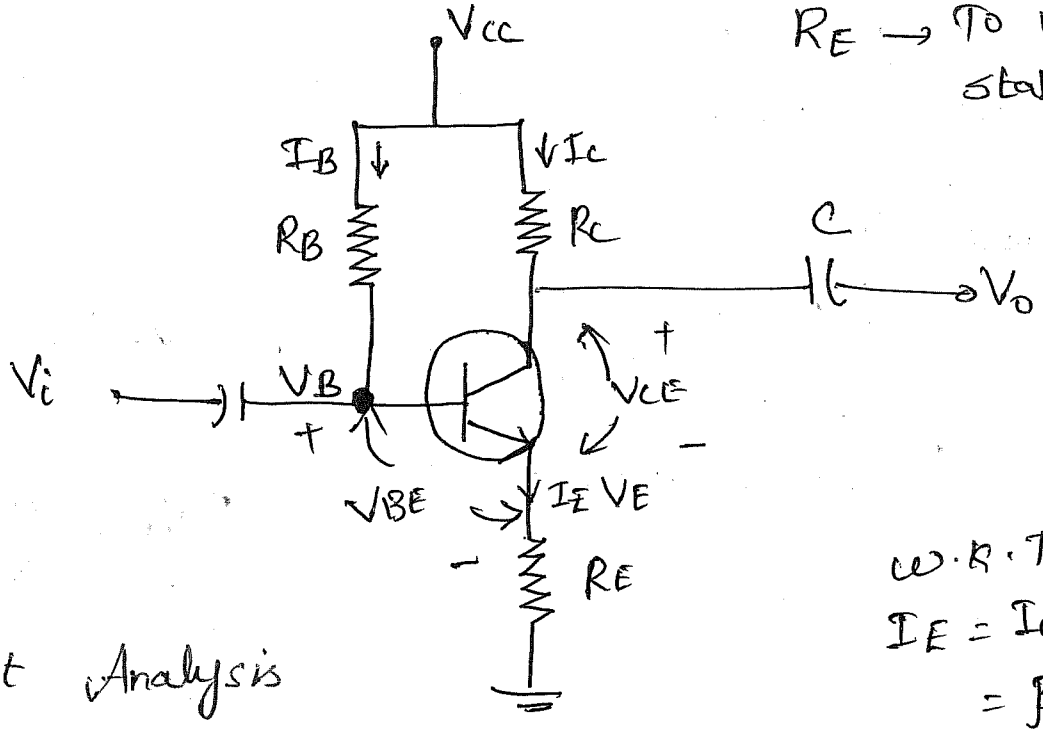
$$S'' = \frac{I_{C1} \cdot S_2}{\beta_1 (1+\beta_2)}$$

$$S_2 = S' = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E} \quad \text{when } \beta = \beta_2.$$

$$\Delta\beta = \beta_2 - \beta_1$$

EMITTER STABILIZED BIAS CIRCUIT

* To improve the stability of the biasing circuit over fixed bias circuit the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as emitter Bias Circuit.



$R_E \rightarrow$ To improve stability.

W.K.T

$I_E = I_C + I_B$

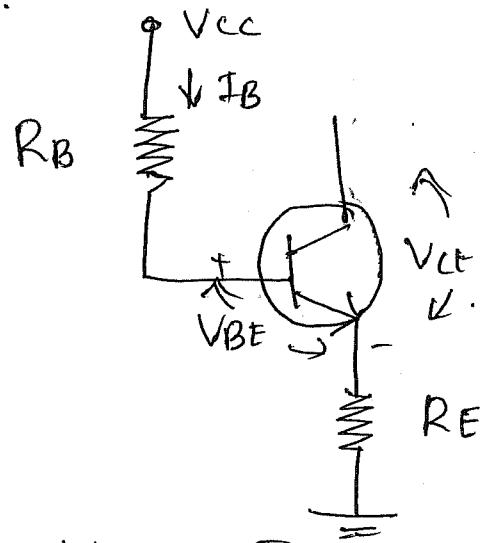
$= \beta I_B + I_B$

$= I_B(\beta+1)$

$I_E = (1+\beta) I_B$

Circuit Analysis

Base Circuit:



$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$

$V_{CC} - V_{BE} = I_B R_B + (1+\beta) I_B R_E$

$$I_B[R_B + (1+\beta)R_E] = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}}$$

$\beta >> 1$

The only difference between fixed bias & emitter stabilized bias is the term βR_E

Apply KVL,

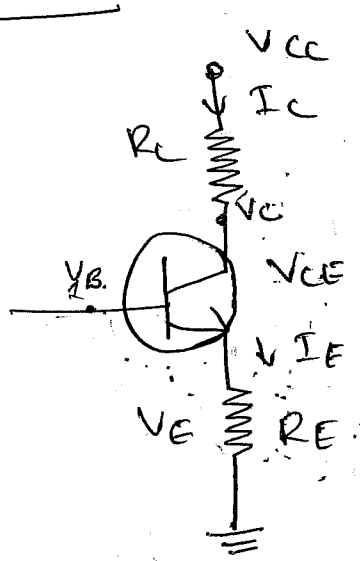
$$V_B - V_{BE} - V_E = 0$$

$$V_B = V_{BE} + V_E \quad \& \quad V_E = I_E R_E$$

$$\boxed{V_B = V_{BE} + I_E R_E}$$

$$\boxed{\begin{aligned} V_B &= V_{BE} + V_E \\ V_C &= V_{CE} + V_E \quad -(1) \end{aligned}}$$

Collector circuit



$$V_B = V_{BE} + V_E$$

$$\boxed{\begin{aligned} V_C &= V_{CC} - I_C R_C \\ V_B &= V_{CC} - I_B R_B \end{aligned}}$$

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore I_C R_C = V_{CC} - V_{CE} - I_E R_E = 0$$

$$I_C R_C = V_{CC} - V_{CE} - I_E R_E$$

$$I_C R_C = V_{CC} - V_{CE} - I_E R_E$$

$I_C = I_E$,

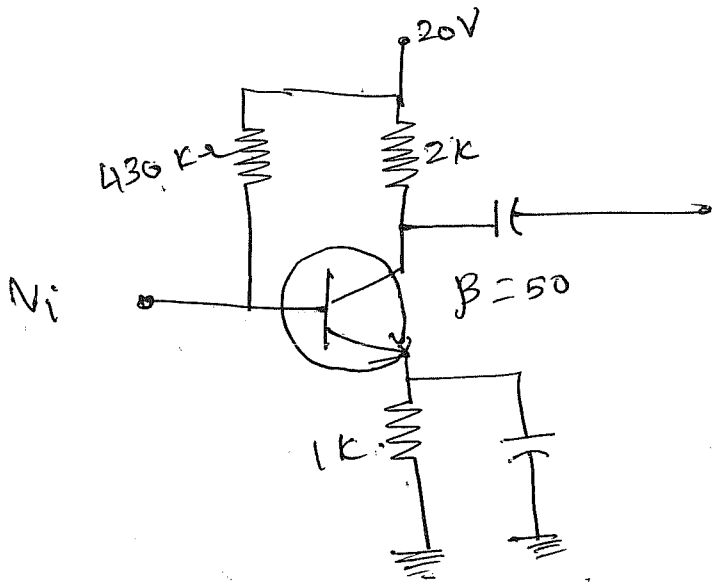
$$I_C R_C = V_{CC} - V_{CE} - I_C R_E$$

$$V_{CE} = V_{CC} - I_C R_E - I_C R$$

$$V_{CE} = V_{CC} - I_C(R_E$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C +}$$

Pb For the emitter bias network determine I_B, I_C V_{CE}, V_C, V_E, V_B and V_{BE}.



Soln

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{20 - 0.7}{430\,k + (1+50) \times 1 \times 10^3}$$

$$\boxed{I_B = 40.125\ \mu A}$$

$$I_C = \beta I_B$$

$$= 50 \times 40.125\ \mu A = 2.00625\ mA.$$

$$\boxed{I_C = 2.00625\ mA}.$$

$$I_E = I_B + I_C = 40.125\ \mu A + 2.00625\ mA$$

$$I_E = 2.046375\ mA.$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = 20 - 2.00625 \times 2K - (2.046375\ mA \times 1K)$$

$$V_{CE} = 13.94\ V$$

$$V_C = V_{CC} - I_C R_C$$

$V_C = 20 - 2.00625mA \times 2K$

$V_C = 15.9875\ V$

$V_E = I_E R_E = 2.046375mA \times 1K$

$V_E = 2.046375\ V$

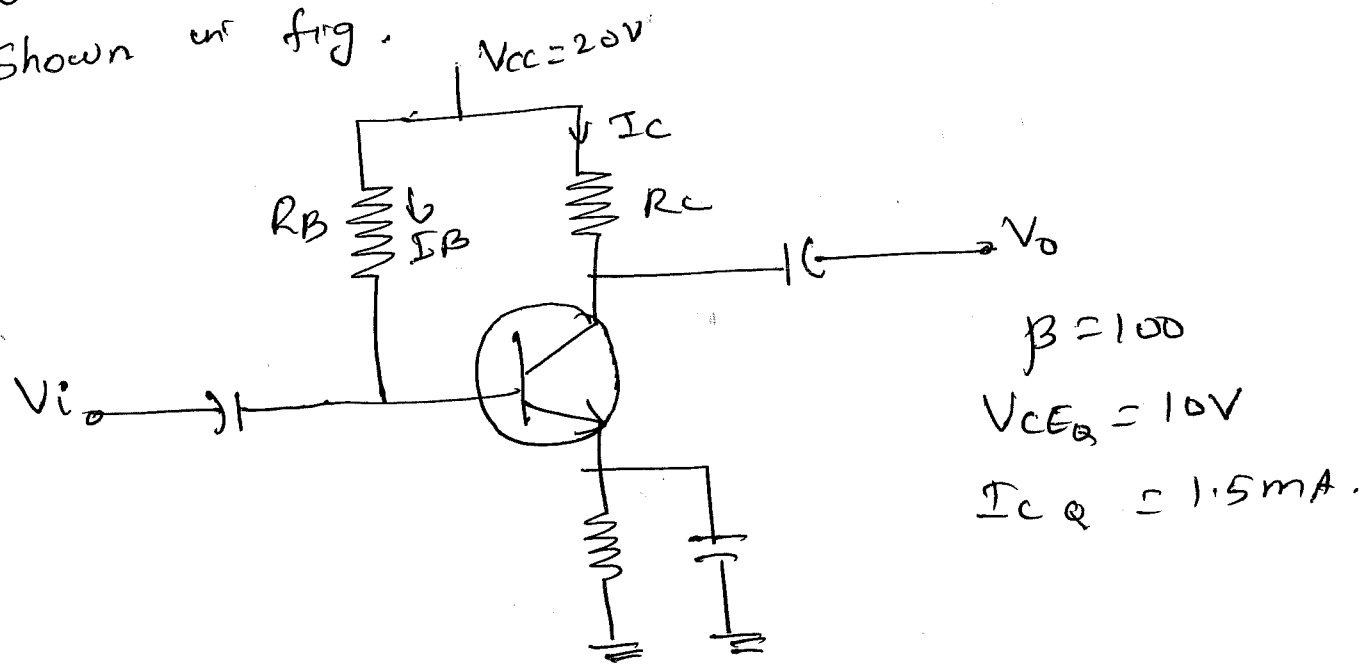
$V_B = V_E + V_{BE} = 2.046375 + 0.7$

$V_B = 2.746375\ V$

$V_{BC} = V_B - V_C = 2.746375 - 15.9875$

$\boxed{V_{BC} = -13.241125\ V}$

Pb Determine the resistor values of the circuit shown in fig.



Let us assume $V_E = \frac{1}{10}$ of V_{CC},

$V_E = 2V$,

$$I_B = \frac{I_C}{\beta} = \frac{1.5\ mA}{100} = 15\ \mu A.$$

$$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C + I_B} = \frac{2}{15MA + 1.5mA}$$

$$R_E = 1.32\ K$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 - 10 - 2}{1.5 \times 10^{-3}}$$

$$R_C = 5.33 *$$

$$R_B = \frac{V_{CC} - V_{BE} - V_E}{I_B}$$

$$= \frac{20 - 0.7 - 2}{15 \times 10^{-6}}$$

$$R_B = 1.15\ M\Omega.$$

EX Design emitter bias for BJT with $I_C = 2mA$, $V_{CC} = 18V$, $V_{CE} = 10V$ and $\beta = 150$.

Soln

Step :1

Obtain I_B and I_E

$$I_B = \frac{I_C}{\beta} = \frac{2mA}{150} = 1333\ \mu A.$$

$I_E = I_B + I_C$

$I_E = 13.33\,\mu A + 2\,mA$

$I_E = 2.0133\ mA.$

Step: 2

Obtain R_E and R_C

$$R_E = \frac{V_E}{I_E} = \frac{1.8\ V}{2.0133\ mA}$$

$R_E = 894\ \Omega$

$V_E = 1.8\ V$

$V_E = \frac{1}{10} V_{CC}$

$V_E = \frac{1}{10} \times 18$

$\boxed{V_E = 1.8\ V}$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$R_C = \frac{18 - 10 - 1.8}{2\,mA}$$

$\boxed{R_C = 3.1\,K}$

Step: 3

Calculate R_B

$R_B = V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0.$

$I_C R_C = V_{CC} - V_{CE} - I_E R_E$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$R_C = \frac{18 - 10 - 1.8}{2\,mA} = 3.1\,k$$

$\boxed{R_C = 3.1\,K}$

Step:3 Calculate R_B

$$R_B = \frac{V_{CC} - V_{BE} - I_E R_E}{I_B}$$

V_E

$$R_B = \frac{18 - 0.7 - 1.8}{13.33\ \mu A}$$

$$R_B = 1.16\ M\Omega$$

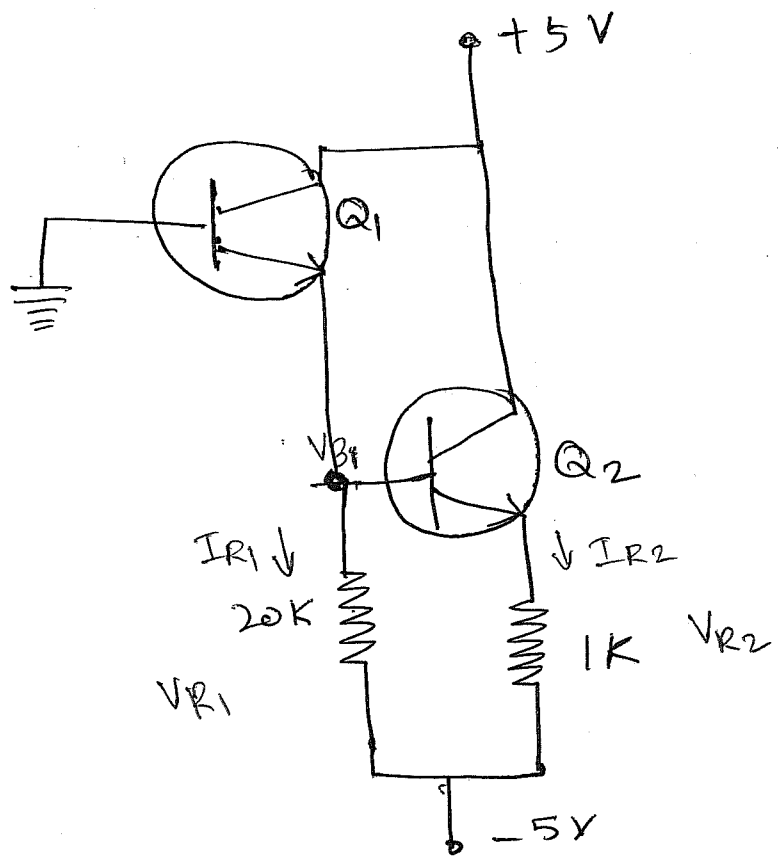
$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - V_{BE} - I_E R_E = I_B R_B$$

$$R_B = \frac{V_{CC} - V_{BE} - I_E R_E}{I_B}$$

$$R_B = \frac{V_{CC} - V_{BE} - V_E}{I_B}$$

(Pb) The Parameters for each transistor in the circuit are $h_{fe} = 100$, $V_{BE(ON)} = 0.7\ V$. Determine the Q Point values of base, Collector and emitter currents in Q_1 and Q_2.



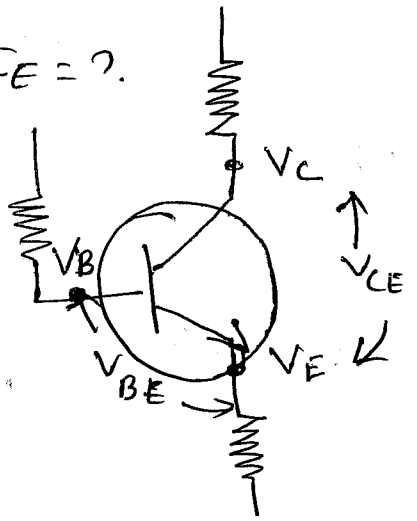
$I_{R2} = I_{E2}$

Given

h_{fe} each = 100, $V_{BE(on)}$ each = 0.7 V

To find

Q point = ?. I_B, I_C, I_E = ?.



Solution.

For the given problem,

$V_{B_1} = V_{BE_1} + V_{E_1}$

$V_{BE_1} = V_{B_1} - V_{E_1}$

$0.7 = 0 - V_{E_1}$

$-V_{E_1} = 0.7$

$\boxed{V_{E_1} = -0.7}$

Now $\boxed{V_{E_1} = V_{B_2}}$

$V_B = V_{BE} + V_E$

$\boxed{V_{BE} = V_B - V_E}$

$V_C = V_{CE} + V_E$

$\boxed{V_{CE} = V_C - V_E}$

$V_{B2} = V_{BE2} + V_{E2}$

$V_{BE2} = V_{B_2} - V_{E2}$

But $V_{B_2} = V_{E1}$ (from the dia, Output of Emitter Voltage of transistor 1 is given as the input base Voltage of transistor). Hence $V_{E_1} = V_{B2}$.

$V_{BE_2} = \overbrace{V_{E_1}}^{V_{B_2}} - V_{E2}$

$V_{BE_2} = -0.7 - V_{E2}$

$0.7 = -0.7 - V_{E2}$

$0.7 + 0.7 = -V_{E2}$

$\boxed{V_{E_2} = -1.4\ V.}$

$V_{R_1} = \dfrac{V_{B_1} - V_{CC}}{R_1}$

$V_{R_1} = \dfrac{V_{E_1} - (-5)}{20K}$

$I_{R1} = \dfrac{V_{R1}}{R_1} = \dfrac{V_{E_1} - V_{CC}}{R_1} = \dfrac{-0.7 - (-5)}{20K} = \dfrac{-0.7+5}{20K}$

$\boxed{I_{R_1} = 0.215\ mA}$

$$I_{E_2} = \frac{V_{E_2} - V_{CC}}{R_2} = \frac{-1.4V - (-5V)}{1k} = \frac{-1.4 + 5V}{1k}$$

$$\boxed{I_{E2} = 3.6mA}$$

$I_{E_2} = (1+\beta)\, I_{B_2}$

To find $I_{B_2} = ?$

$$\boxed{I_{B_2} = \frac{I_{E_2}}{1+\beta}}$$

$I_E = I_C + I_B$

$I_E = \beta I_B + I_B$

$I_E = (1+\beta) I_B$

$$I_{B_2} = \frac{3.6mA}{1+100} = 0.03564\ mA$$

$$\boxed{I_{B_2} = 0.03564\ mA}$$

$$I_{C_2} = \beta I_{B_2} = 100 \times 0.03564\ mA$$

$$\boxed{I_{C_2} = 3.564\ mA}$$

$$I_{E_1} = I_{R_1} + I_{B_2} = 0.215 + 0.03564$$

$$\boxed{I_{E_1} = 0.25\ mA}$$

$$I_{B_1} = \frac{I_{E_1}}{1+\beta} = \frac{0.25mA}{1+100} = \frac{0.25mA}{101}$$

$$\boxed{I_{B1} = 0.00248\ mA.}$$

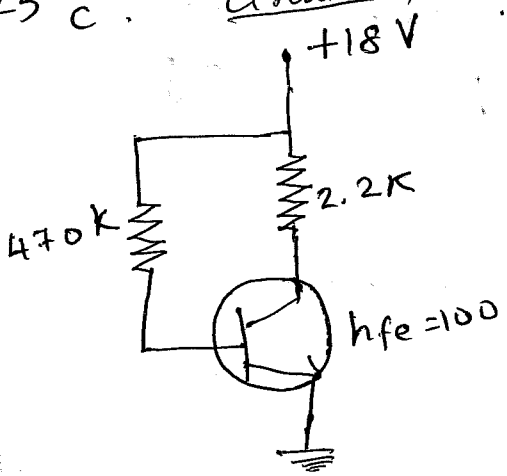
$I_{C_1} = \beta I_{B_1}$

$= 100 \times 0.00248$

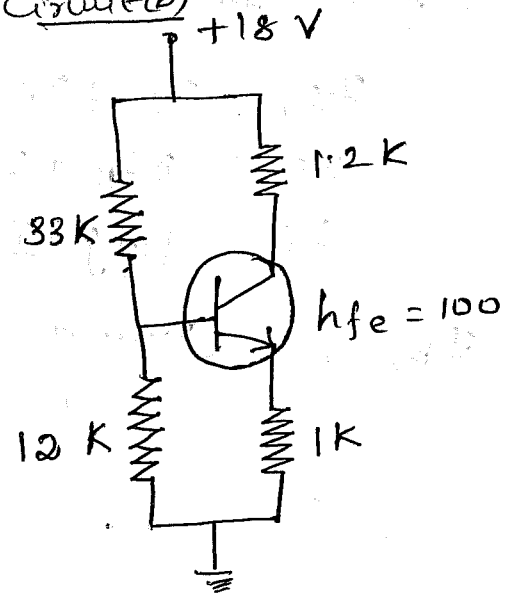
$$\boxed{I_{C_1} = 0.248\ mA}$$

Pb Determine the change in Collector current produced in each bias referred to following circuits (a) and (b), when the circuit temperature raised from 25°C to 105°C and $I_{CO} = 15\,nA$ @ 25°C.

Circuit (a)



Circuit (b)



For fixed bias circuit

$S = 1 + \beta$, for circuit a,

$S = 1 + 100$

$S = 101$

$\Delta I_C = S \cdot \Delta I_{CBO}$

W.K.T

$S = \frac{\partial I_C}{\partial I_{CO}}$

$\partial I_C = S \cdot \partial I_{CO}$

$\Delta I_C = S \cdot \Delta I_{CO}$

$\Delta I_C = S \cdot \Delta I_{CBO}$

Given

$I_{CBO} = 15\,nA$ @ 25°C.

To find

change in I_C ?. for each bias.

Soln

$\Delta I_C = S \cdot \Delta I_{CBO}$

$S = 101$

$\Delta I_{CBO} = I_{CBO2} - I_{CBO1}$

[. Change in or difference in I_{CBO}]

$$I_{CBO_2} = I_{CBO_1} \cdot 2^{n} \qquad n = \frac{T_2 - T_1}{10}$$

$$n = \frac{T_2 - T_1}{10} = \frac{105 - 25}{10} = 8$$

$n = 8$

$I_{CBO_1} = 15\,nA$ @ $25^\circ C$

$$I_{CBO_2} = (15\,nA) \times 2^{8}$$

$$\boxed{I_{CBO_2} = 3.84\,\mu A}$$

$$\Delta I_{CBO} = I_{CBO_2} - I_{CBO_1}$$

$$= 3.84\,\mu A - 15\,nA$$

$$\boxed{\Delta I_{CBO} = 3.83\,\mu A}$$

$$\Delta I_C = S \cdot \Delta I_{CBO}$$

$$= (101)(3.83\,\mu A)$$

$$\boxed{\Delta I_C = 383.6}$$

For Voltage divider Bias Circuit,

$$S = \frac{1+\beta}{1 + \frac{\beta R_E}{R_E + R_B}}$$

where $R_B = \frac{R_1 R_2}{R_1 + R_2}$

$$R_B = \frac{33K \times 12k}{33K + 12k}$$

$$\boxed{R_B = 8.8K}$$

$\beta = 100$

$R_E = 1k$

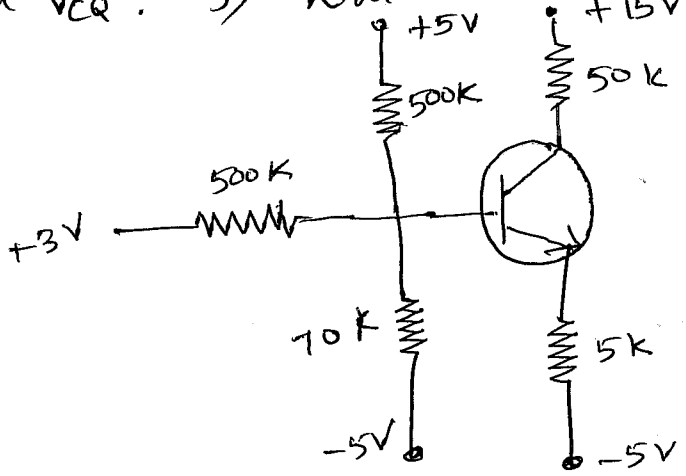
$$S = \frac{1+100}{1 + \frac{100 \times 1K}{1K + 8.8K}}$$

$S = 9.01$

$$\Delta I_C = S \times \Delta I_{CO} = 9.01 \times 3.83\,\mu A$$

$$\Delta I_C = 34.51\,\mu A.$$

5h The Circuit in the fig let h_{fe} = 100, Find V_{TH}, R_{TH} for the base circuit. Determine I_{CQ} and V_{CQ}. 3) Draw the DC load line.



Soln

Given $h_{fe} = 100$.

To find

V_{TH}, R_{TH}, I_{CQ}, V_{CQ} & DC load line.

$$R_{TH} = 500K \,||\, 500K \,||\, 70K$$

$$= R_B \quad \frac{500K \times 500K}{500K + 500K} \,||\, 70K$$

$$= 250K \,||\, 70K = \frac{250K \times 70K}{250K + 70K}$$

$$\boxed{R_{TH} = 54.7K = R_B}$$

Apply KCL,

$$\frac{5 - V_{TH}}{500} + \frac{3 - V_{TH}}{500} + \frac{(-5) - V_{TH}}{70} = 0$$

$$\frac{5 - V_{TH}}{500K} + \frac{3 - V_{TH}}{500K} - \frac{5 - V_{TH}}{70K} = 0$$

$$\frac{5}{500K} - \frac{V_{TH}}{500K} + \frac{3}{500K} - \frac{V_{TH}}{500K} - \frac{5}{70K} - \frac{V_{TH}}{70K} = 0$$

$$\frac{5}{500k} + \frac{3}{50K} - \frac{5}{70K} = \frac{V_{TH}}{500K} + \frac{V_{TH}}{500K} + \frac{V_{TH}}{70K}$$

$$-0.0554 \times 10^{-3} = V_{TH}\left(\frac{1}{500K} + \frac{1}{50K} + \frac{1}{70K}\right)$$

$$-0.0554 \times 10^{-3} = V_{TH}\,(0.0183 \times 10^{-3})$$

$$V_{TH}(0.0183) = -0.0554$$

$$\boxed{V_{TH} = -3.03\ V}$$

Base current for Voltage divider circuit.

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$I_B = \frac{-3.03 - 0.07 - (-5)}{54.7 + (1+100)\,5K}$$

$$\boxed{I_B = 0.00227\ mA}$$

$$I_C = \beta I_B$$

$$= 100 \times 0.00227\ mA$$

$$\boxed{I_C = 0.227\ mA.}$$

$$I_E = I_B + I_C = 0.00227\ mA + 0.227\ mA$$

$$\boxed{I_E = 0.229\ mA}$$

Apply KVL,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E - (-V_{EE}) = 0$$

$$V_{CE} = V_{CC} - (-V_{EE}) - I_C R_C - I_E R_E$$

$$= 15 - (-5) - (0.227 \times 50) - (0.229 \times 5)$$

$$V_{CE} = 15 + 5 - (0.227 \times 50) - (0.229 \times 5)$$

$$\boxed{V_{CE} = 7.51\ V}$$

(ii) Dc Load Line

Point A

$$V_{CE} = V_{CC} - (-V_{EE})$$

$$= 15 - (-5)$$

$$\boxed{V_{CEQ} = 20V} \quad @ \quad I_C = 0$$

Point B

$$I_C = \frac{V_{CC} - (-V_{EE})}{R_C + R_E}$$

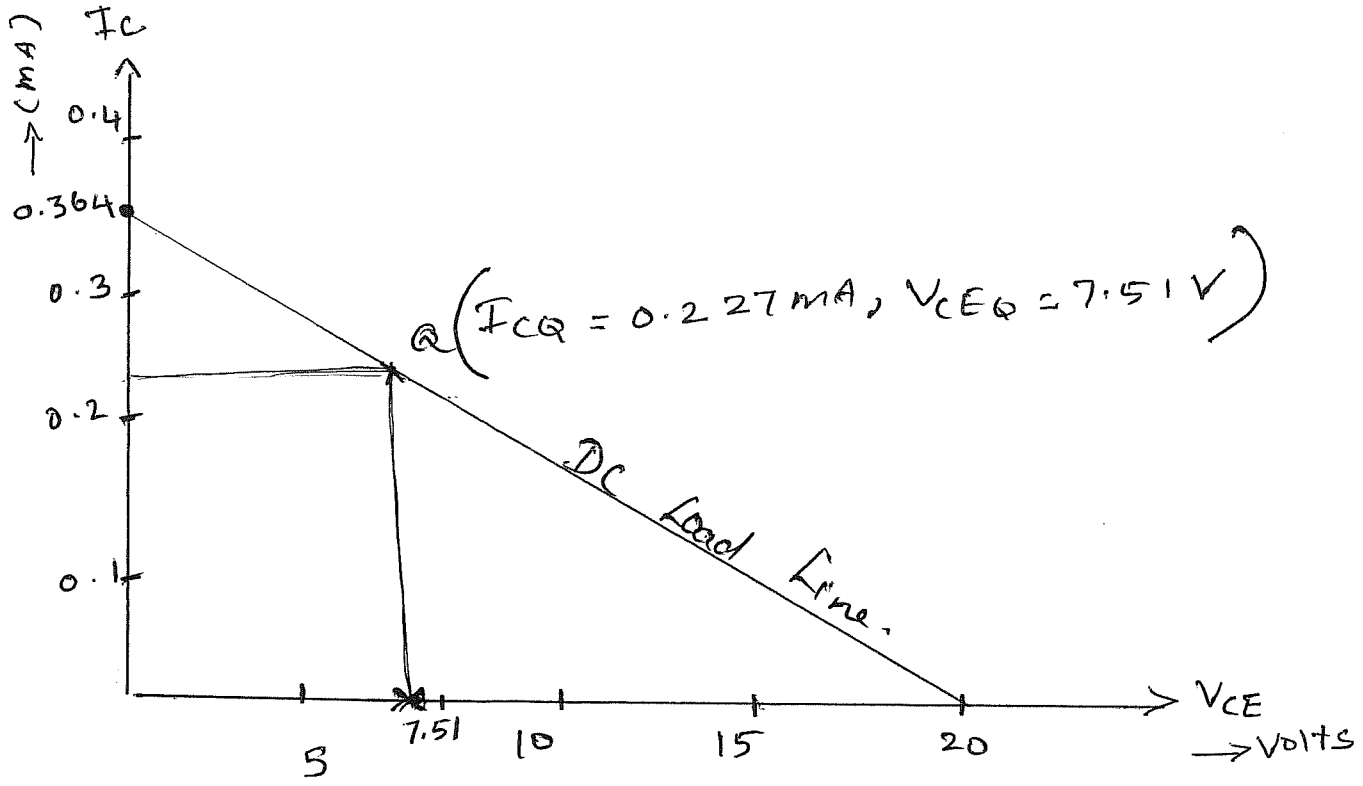
$$I_C = \frac{15 - (-5)}{50K + 5K} = \frac{15 + 5}{50K + 5K}$$

$$I_{CQ} = \frac{20}{50K + 5K}$$

$$\boxed{I_C = 0.364\ mA}$$

Operating Point = (V_{CEQ}, I_{CQ})

Operating Point = $(20V, 0.364\ mA)$



Ans:

$V_{TH} = -3.03\ V$

$I_B = 0.00227\ mA.$

$I_C = 0.227\ mA$

$I_E = 0.229\ mA$

$V_{CE\,Q} = 7.51\ V$

Point A = 20V @ $I_C = 0$

Point B = 0.364

Bias Compensation.

The different types of biasing circuits are used to provide stability of operating point in case of variation in transistor parameters such as I_{CO}, V_{BE} and β. The collector to base bias and voltage follower bias use the negative feedback due to the stabilization action.

This negative feedback reduces amplification of the signal. So this loss in signal amplification is intolerable.

Hence extremely stable biasing conditions are required. Hence it is necessary to use Compensation techniques.

* The Compensation techniques use temperature sensitive devices such as diodes, transistors, termistors etc to maintain operating point constant. Three compensation techniques are in general used.

1. Diode Compensation Technique.
2. Thermistor Compensation Technique
3. Sensistor Compensation Technique.

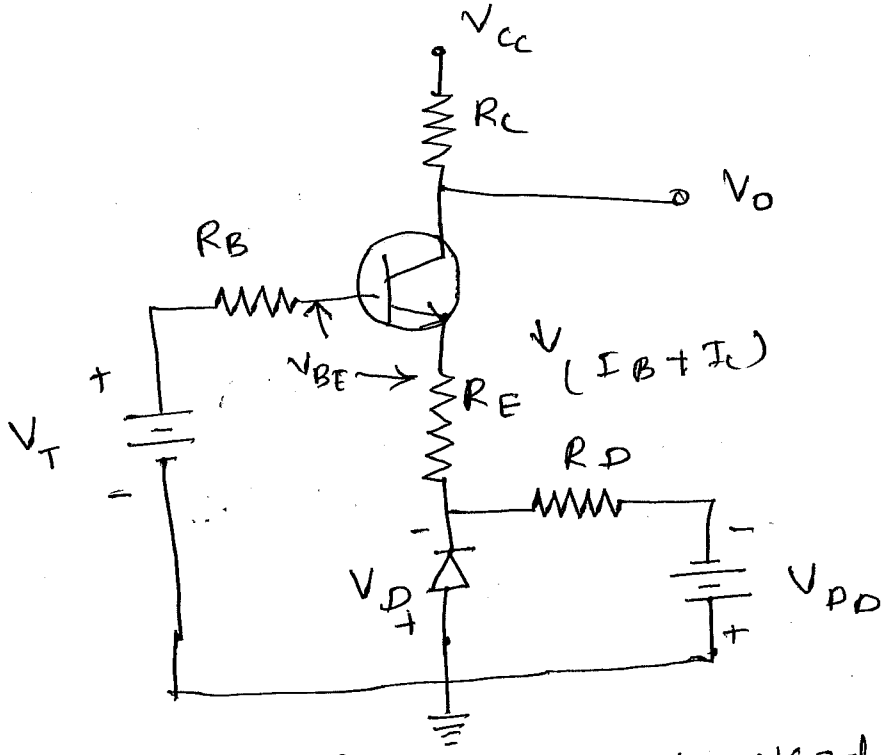
1. Diode Compensation Techniques:

Compensation for V_{BE}:

a) Diode in Emitter circuit:

Consider a Voltage divider bias circuit.

with bias Compensation technique.



Separate supply V_{DD} is used to keep diode in forward biased condition. If the circuit used with the diode has the same material type as the transistor the voltage across the diode will have the same temperature co-efficient (−2.5mV/°C) because of the base emitter voltage V_{BE}.

So when V_{BE} is changes by ∂V_{BE} with change in temperature V_D changes by ∂V_D and

$$\partial V_D = \partial V_{BE}$$

and the changes tend to cancel each other.

Apply KVL, to the base circuit,

$$V_{TH} - I_B R_B - V_{BE} - (I_B + I_C) R_C + V_D = 0$$

$$V_{TH} = I_B R_B + V_{BE} + \underbrace{(I_B + I_C)}_{I_E} R_E - V_D$$

$$= I_B R_B + V_{BE} + \boxed{I_B R_E + I_C R_E} - V_D$$

$$= I_B R_B + V_{BE} + I_B R_E - V_D + I_C R_E$$

$$= I_B (R_B + R_E) + I_C R_E + V_{BE} - V_D$$

$$V_{TH} = I_B(R_B + R_E) + I_C R_E + V_{BE} - V_D \quad \text{——①}$$

Considering the leakage Currents,

$$I_B = \frac{I_C}{\beta}$$

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$I_C = \beta \left(\frac{I_C}{\beta}\right) + (1+\beta) I_{CO}$$

÷ by β both LHS & RHS of the equation

$$\frac{I_C}{\beta} = \frac{\beta}{\beta}\frac{I_C}{\beta} + \frac{(1+\beta)}{\beta} I_{CO}$$

$$\frac{I_C}{\beta} = \frac{I_C}{\beta} + \frac{(1+\beta)}{\beta} I_{CO}$$

$$I_B = \frac{I_C}{\beta} + \frac{(1+\beta)}{\beta} I_{CO}$$

Substituting the value of I_B in ①,

① ⇒

$$V_{TH} = I_B(R_B + R_E) + I_C R_E + V_{BE} - V_D$$

$$V_{TH} = \underbrace{\left(\frac{I_C}{\beta} + \frac{(1+\beta) I_{CO}}{\beta}\right)}_{I_B}(R_B + R_E) + I_C R_E + V_{BE} - V_D$$

$$V_{TH} = \frac{I_C}{\beta}(R_B + R_E) + \frac{(1+\beta) I_{CO}(R_B + R_E)}{\beta} + \frac{\beta}{\beta} I_C R_E + V_{BE} - V_D$$

$$V_{TH} = \frac{I_C}{\beta}(R_B + R_E) + \frac{\beta}{\beta} I_C R_E + \frac{(1+\beta) I_{CO}(R_B + R_E)}{\beta} + V_{BE} - V_D$$

$$= \frac{I_C}{\beta} R_B + \frac{I_C}{\beta} R_E + \frac{\beta}{\beta} I_C R_E + \frac{(1+\beta) I_{CO}(R_B + R_E)}{\beta} + V_{BE} - V_D$$

$$= \frac{I_C}{\beta}(R_B + R_E + \beta R_E) + \frac{(1+\beta) I_{CO}(R_B + R_E)}{\beta} + V_{BE} - V_D$$

$$= \frac{I_C}{\beta}(R_B + R_E(1+\beta)) + \frac{(1+\beta) I_{CO}(R_B + R_E)}{\beta} + V_{BE} - V_D$$

$$V_{TH} = \frac{I_C}{\beta}\left[R_B + (1+\beta) R_E\right] + \frac{(R_B+R_E)(1+\beta) I_{CO} + V_{BE} - V_D}{\beta}$$

$$V_{TH} - V_{BE} + V_D = \frac{I_C}{\beta}\left[R_B + (1+\beta) R_E\right] + \frac{(R_B+R_E)(1+\beta) I_{CO}}{\beta}$$

$$V_{TH} - V_{BE} + V_D + (R_B + R_E)(1+\beta) I_{CO} = \frac{I_C}{\beta}\left[R_B + (1+\beta) R_E\right]$$

because of Reverse leakage current very less

$$\frac{I_C}{\beta}\left[R_B + (1+\beta) R_E\right] = V_{TH} - V_{BE} + V_D + \frac{(R_B+R_E)(1+\beta) I_{CO}}{\beta}$$

$$I_C\left[R_B + (1+\beta) R_E\right] = \frac{\beta V_{TH} - \beta V_{BE} + \beta V_D + (R_B+R_E)(1+\beta) I_{CO}}{\beta}$$

$$I_C\left[R_B + (1+\beta) R_E\right] = \beta\left[V_{TH} - V_{BE} + V_D\right] + (1+\beta)(R_B+R_E) I_{CO}$$

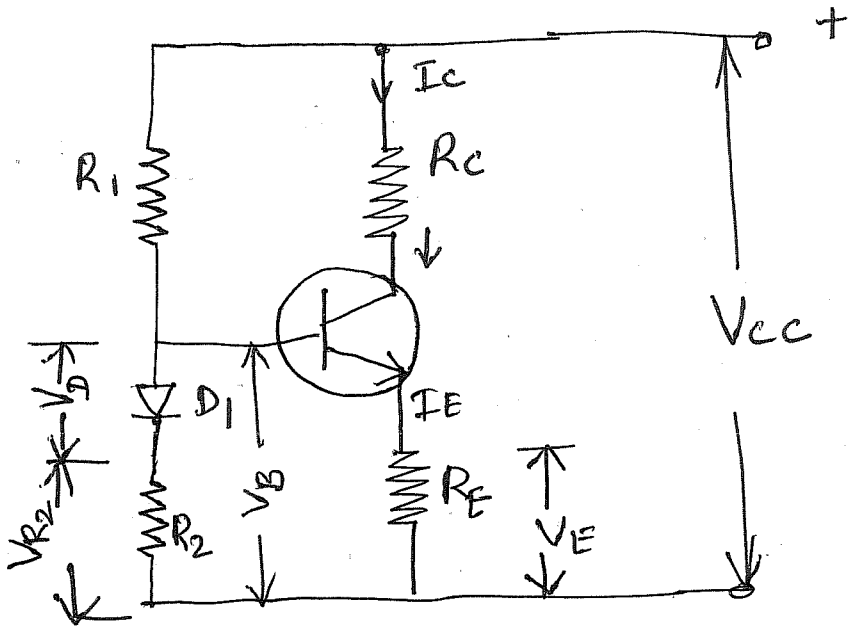
$$I_C\left[R_B + (1+\beta) R_E\right] = \beta\left[V_{TH} - (V_{BE} - V_D)\right] + (1+\beta)(R_B+R_E) I_{CO}$$

$$I_C = \frac{\beta\left[V_{TH} - (V_{BE} - V_D)\right] + (1+\beta)(R_B+R_E) I_{CO}}{R_B + (1+\beta) R_E}$$

Since V_D tracks V_{BE} with respect to temperature, it is clear that I_C will be insentive to Variations in V_{BE}.

b) DIODE IN VOLTAGE DIVIDER CIRCUIT [I_C Compensation]

Let us Consider the diode compensation technique used in Voltage divider Bias. Here the diode is connected in series with the resistance R_2 in the voltage divider circuit and it is forward biased Condition.



We know that from voltage divider circuit the emitter current I_E is given by,

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{V_E}{R_E}$$

When $I_C \approx I_E$, I_C is also given by,

$$I_C = \frac{V_B - V_{BE}}{R_E}$$

When V_{BE} changes with temperature, I_C also changes. To cancel the change in I_C, one diode is used in this circuit for compensation.

The voltage at the base V_B is now

$$V_B = V_{R2} + V_D$$

Subs, the value of V_B in I_C expression,

$$I_C = \frac{V_B - V_{BE}}{R_E} = \frac{(V_{R2} + V_D) - V_{BE}}{R_E}$$

$$I_C = \frac{V_{R_2} + V_D - V_{BE}}{R_E}$$

If the diode which is used in this circuit is of same material and type as the transistor the voltage across the diode will have the same temperature co-efficient ($-2.5\ mV/^{\circ}C$) as the base to emitter voltage is V_{BE}.

So when V_{BE} changes by ∂V_{BE} with the change in temperature V_D changes by ∂V_D and $\partial V_D \approx \partial V_{BE}$, the changes tends to cancel other and leave the collector current as,

$$I_C = \frac{V_{R2}}{R_E}$$

∴ $I_C = \frac{V_{R_2} + V_D - V_{BE}}{R_E}$

$\partial V_D \approx \partial V_{BE}$,

$I_C = \frac{V_{R2} + V_D - V_E}{R_E}$

$I_C = \frac{V_{R2}}{R_E}$

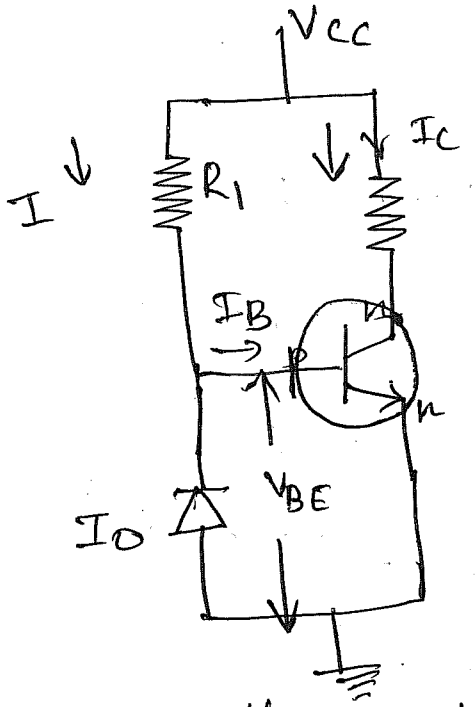
* This collector current is unaffected due to the change in V_{BE}.

In this circuit we know that biasing is provided by R_1, R_2 and R_E. The change in V_{BE} due to temperature are compensated by changes in diode voltage keeping I_C stable at Q point.

(C) **Compensation for I_{CO}**

In case of germanium transistors, changes in I_{CO} with temperature are comparatively larger than silicon transistor.

Thus for a germanium transistor changes in I_{CO} with temperature play more important role in collector current stability than the changes in V_{BE}. Figure shows the diode compensation technique commonly used for stabilizing germanium transistors.



The circuit offers stabilization against variation of I_{CO}. In this circuit diode is kept under reverse biased condition. In reverse biased condition the current flow through the diode is only the leakage current. If the diode and the transistor are of the same type and material the leakage current I_O of the diode will increase with temperature as the same rate as the collector leakage current I_{CO}.

from the fig,

$$I = \frac{V_{CC} - V_{BE}}{R_1}$$

$I = I_B + I_O$ $\Rightarrow$ $I_B = I - I_O$

For germanium transistor $V_{BE} = 0.2\,V$ and which is very small and neglecting change in V_{BE} with temperature.

$V_{BE} = 0.2$, and there is neglecting change in V_{BE}. Hence neglect V_{BE}.

$$I = \frac{V_{CC}}{R_1}$$

$$I = \frac{V_{CC}}{R_1} \text{ [constant]}$$

We know that,

$$I_C = \beta I_B + (1+\beta) I_{CO}.$$

Substituting the value of I_B in the above eqn,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta (I - I_O) + (1+\beta) I_{CO} \qquad (1+\beta) \div \beta$$

$$I_C = \beta I - \beta I_O + \beta I_{CO}$$

If $I_O = I_{CO}$ we get

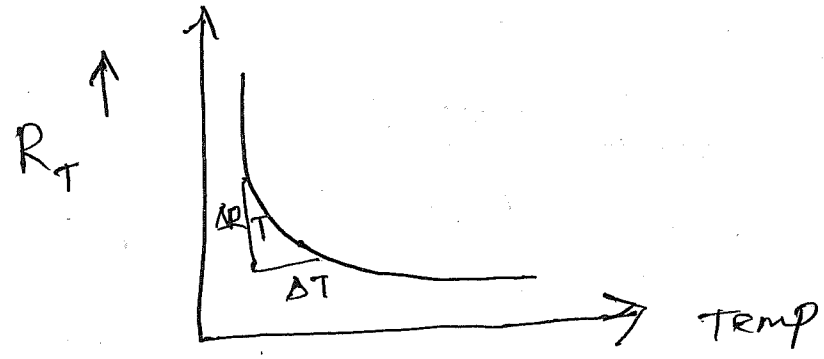
$$I_C = \beta I - \beta I_{CO} + \beta I_{CO}$$

$$\boxed{I_C = \beta I}$$

As I is Constant, I_C remains finally Constant. i.e) the charges by I_{CO} with temperature are Compensated by diode and thus the Collector Current remains Constant.

THERMISTOR COMPENSATION

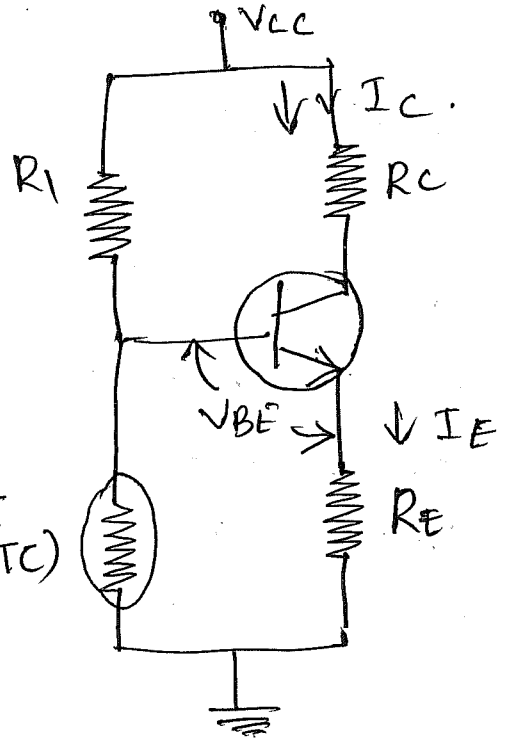
This method of transistor compensation uses temperature sensitive elements, termistors rather than diodes or transistors. It has a negative temperature co-efficient (NTC) Its resistance decreases exponentially with increase in temperature.



Slope of this curve is

$$\frac{\partial R_T}{\partial T}.$$

The expression $\frac{\partial R_T}{\partial T}$ is called as the temperature co-efficient of termistor.



Negative Temp. Coefficient

Figure shows the termistor compensation technique. R_2 is replaced by thermistor R_T. in Self bias / Voltage divider bias circuit.

With increase in temperature, R_T decreases. This voltage drop is nothing but the voltage at the base with respect to ground.

Hence V_{BE} decreases with decrease in I_B. So that the increase in collector current will be balanced with temperature.

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

* To the equation there is increase in I_{CO} and decrease in I_B which keeps I_C constant
* Consider another thermistor connected between emitter and V_{CC} to minimize the increase in collector current, due to the change in I_{CO}, V_{BE} or β with temperature
* I_C increase with temperature and R_T decreases with increase in Temperature Temp ↑, I_C ↑ R_T ↓
* therefore current flowing through the R_E also increases, which increases the voltage drop across it.
* E-B. junction is forward biased.
  1) Emitter - Base junction forward biased.
  2) Voltage drop across E-B, V_{BE} ↑↑ increases
  3) ∴ Current flowing through R_E ↑↑ increases.

4) Therefore Increase in V_E, V_E ↑es. (Voltage drop across R_E).

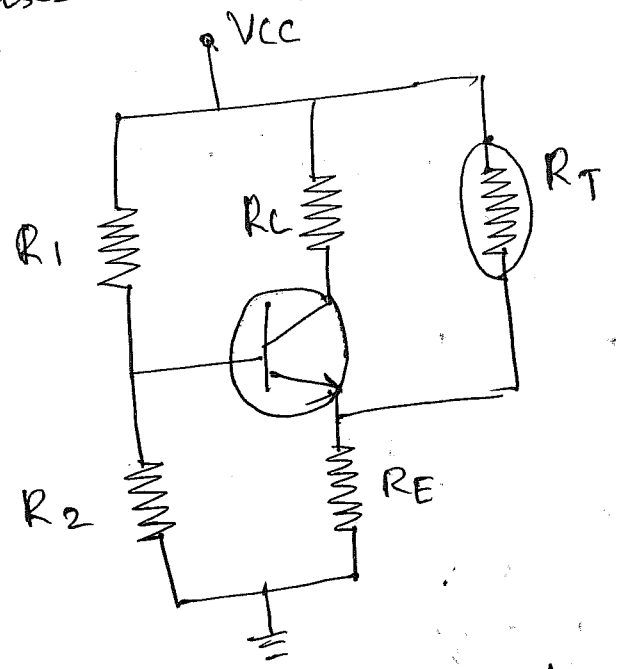
5) Hence emitter is made more positive.

6) This reduces V_{BE}. (R_E ^{CO_2} grounded).

7. Hence Base current reduces.

$$I_C = \beta I_B + (\beta+1) I_{CO}.$$

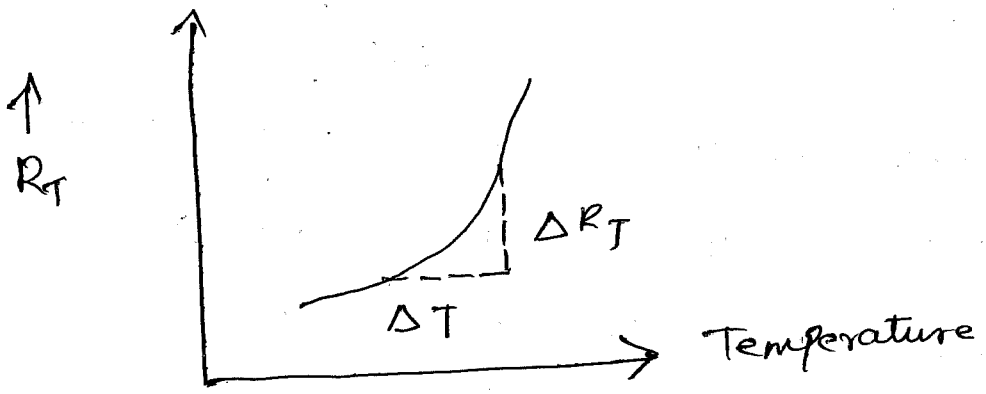
* As I_{CO} increases with temperature I_B decreases.



Hence I_{CO} increases hence I_C remains Constant because of decrease in I_B.

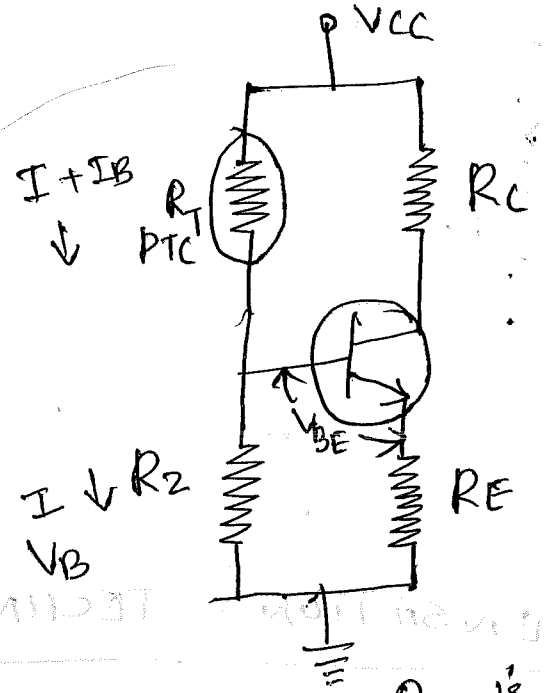
SENSISTOR COMPENSATION TECHNIQUE

This method of transistor compensation uses temperature Sensitive resistive element sensistors rather than diodes or transistors. It has positive temperature (PTC) co-efficient. Its resistance increases exponentially with increasing temperature



Slope of this curve is $\frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature co-efficient of thermistor, and the slope is positive. So we can say that sensitor has positive temperature co-efficient (PTC)



* figure shows R_1 is replaced by Sensistor R_T is self bias or voltage divider bias. Now R_T and R_2 are the two resistors of the potential divider.

* As temperature ↑es R_T ↑es. R_T ↑es → I ↓ (I=I+I current flow through R_T.

I (I+IB) ↓ → IR_2 ↓

* I_{R_2} ↓ es → V_B ↓ V_B = Voltage drop across R_2

Current flow through R_2

* V_{BE} ↓ → I_B ↓

This means when I_{CO} increases with increase in temperature I_B reduces due to the reduction of V_{BE}, maintaining I_C Constant.

THERMAL STABILITY

The maximum power (average) $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction and may lie in the range from ~~200~~ a few milliwatts to 200 W. As we know the power dissipated within the transistor is simply the power dissipated at its Collector - Base junction.

The maximum power is limited by the temp. at the Collector Base junction, is ranges from 150° to 225°C and for germanium it is between 60°C to 100°C.

The Collector Base junction temperature may rise because of the two reasons.

* Due to rise in ambient temperature
* Due to Self heating.

* Self heating is defined as the increase in the collector current increases the power dissipated at the collector junction.

* This in turn further increases the temperature of the junction, and hence again increases the collector current.

* This process cumulative is referred as Self heating.

* The excess heat produced at the collector base junction may even burn and destroy the transistor.

* This situation is called "Thermal runaway" of the transistor.

Thermal Resistance (θ)

The steady state temperature rise at at the collector junction is proportional to the power dissipated at the junction. ie)

$$\partial T = T_j - T_A \quad -①$$

$$\partial T = \theta P_D \quad -②$$

T_j = Junction temp. in °C

T_A = Ambient temp in °C

P_D = Power dissipated at collector junction in watts

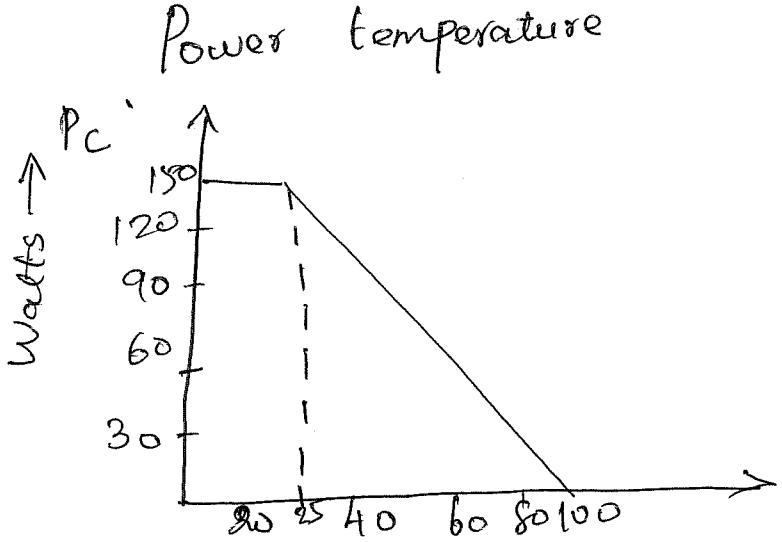
θ = Constant of proportionality ie thermal resistance.

Equating ① & ②,

$$\theta P_D = T_j - T_A \quad -③$$

$$\boxed{\theta = \frac{T_j - T_A}{P_D}}$$

* The unit of thermal resistance θ is given by °c/watt. The values of θ ranges from 0.2 °c/W to 1000 °c/W. The maximum Collector Power P_C allowed for safe operation is 25°c.



* It shows that above 25°c Collector Power must be decreased, and the extreme temperature the transistor may operate P_C is reduced to zero.

The Condition for Thermal Stability

We know that the thermal runaway may even burn and destroy the transistor. So its necessary to avoid thermal runaway.

The required Condition to avoid thermal runaway is " the rate at which heat is released at the collector junction must not exceed the rate at which the heat can dissipated". In the form of equation,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \text{---(4)}$$

Differentiate eqn (3) w.r.t T_j gives,

(3) $\Rightarrow$

$$T_j - T_A = \theta \times P_D$$

diff w.r.t T_j

$$1 - 0 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\boxed{\frac{\partial P_D}{\partial T_j} = \frac{1}{\theta}} \quad \text{---(5)}$$

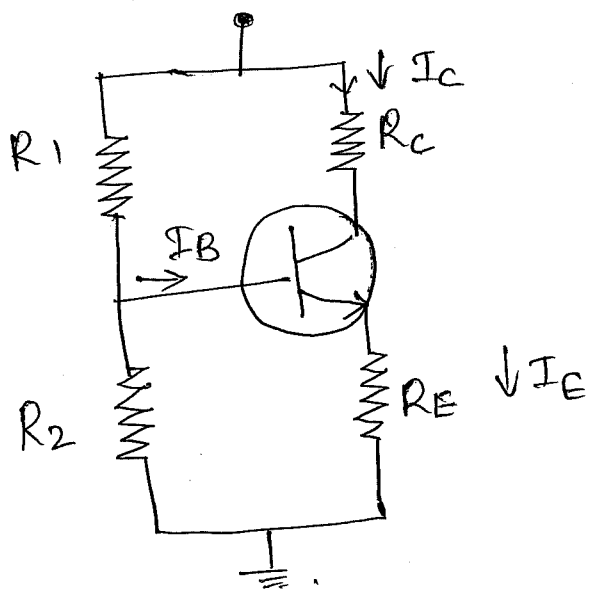
Substituting in (4), $\Rightarrow \frac{1}{\theta}$

$$4 \Rightarrow \frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$$

$$\boxed{\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}} \Leftarrow \text{Condition to avoid Thermal runaway.} \quad \text{---(6)}$$

* By proper design of biasing circuit it is Possible, to avoid thermal runaway.

Lets Consider the divider circuit for analys



Let

P_C = Heat generated at the collector junction.

P_C = DC power input − Power Lost in (R_C & R_E)

P_C Heat generated at P_C } = $V_{CC} \times I_C$ − Power lost in R_C & R_E

Where $V_{CC} \times I_C$ is the DC power input to the Circuit.

Power lost in R_C & R_E is I^2R_C & I^2R_E. So

$$P_C = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E$$

If $I_C = I_E$

$$P_C = V_{CC} \times I_C - I_C^2 R_C - I_C^2 R_E$$

$$P_C = V_{CC} I_C - I_C^2 (R_C + R_E) \quad \text{—— (7)}$$

Differentiating the above expression w.r.t I_C

$$\boxed{\frac{\partial P_C}{\partial I_C} = V_{CC} - 2 I_C (R_C + R_E)} \quad \text{—— (B)}$$

Rewriting the condition for thermal runaway

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \Rightarrow \frac{\partial P_C}{\partial T_j} \times \frac{\partial I_C}{\partial I_C} < \frac{1}{\theta}$$

$$\boxed{\frac{\partial P_C}{\partial I_C} \times \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta}} \quad \text{—— (A)}$$

I_{CO}
V_{BE}
β

$\frac{\partial I_C}{\partial T_j}$ can be written as

$$\frac{\partial I_C}{\partial T_j} = S \frac{\partial I_{CO}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j} \quad \text{—— (8)}$$

As we are doing analysis for Thermal runaway the affect of I_{co} can only be considered.

$$\frac{\partial I_c}{\partial T_j} = \frac{\partial I_{co}}{\partial T_j} \cdot S \qquad \text{—— (9)}$$

As the reverse saturation current for both germanium and silicon increases about 7 percent per °C

$$\frac{\partial I_{co}}{\partial T_j} = 0.07 I_{co} \qquad \text{—— (10)}$$

Substituting the value of $\frac{\partial I_{co}}{\partial T_j}$ in $\frac{\partial I_c}{\partial T_j}$ eqn (9)

$$\frac{\partial I_c}{\partial T_j} = \frac{\partial I_{co}}{\partial T_j} \times S$$

$$\frac{\partial I_c}{\partial T_j} = 0.07 I_{co} \times S \qquad \text{—— (C)}$$

We know that, (A) $\Rightarrow$

$$\frac{\partial P_c}{\partial I_c} \cdot \frac{\partial I_c}{\partial T_j} < \frac{1}{\theta}$$

Substituting the values in the above expression, (B) & (C),

$$V_{cc} - 2 I_c (R_c + R_E) \times S \times 0.07 I_{co} < \frac{1}{\theta}$$

$$V_{cc} < 2 I_c (R + R_E)$$

As, 'S', I_{co} and θ are positive we have

$$V_{cc} < 2 I_c (R_c + R_E)$$

$$\frac{V_{cc}}{2} < I_c (R_c + R_E) \qquad \text{—— (11)}$$

Applying KVL to the collector circuit,

$$V_{CC} - V_{CE} - I_C R_C - I_E R_E = 0$$

$$V_{CC} - V_{CE} = I_C R_C + I_E R_E$$

$$= I_C R_C + (I_C + I_B) R_E \qquad I_C = I_E$$

$$= I_C R_C + I_C R_E + I_B R_E$$

I_B Current Very small neglected.

$$V_{CC} - V_{CE} = I_C (R_C + R_E) \qquad \text{---(12)}$$

(11) & (12) RHS is same. Hence LHS can be

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

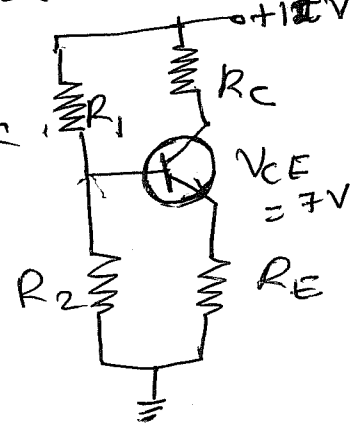
$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$\boxed{V_{CE} < \frac{V_{CC}}{2}} \Leftarrow \text{Condition for thermal stability.}$$

V_{CE} is always selected lesser than $\frac{V_{CC}}{2}$ for thermal stability.

2b Calculate the value of thermal resistance θ for the transistor in the circuit shown in figure, in order to make circuit thermally stable. Assume $I_{CO} = 1nA$ @ $25^\circ C$.

$V_{CC} = +12V$, $R_1 = 100K$, $R_C = 2K$



To find

Thermal resistance θ.

$V_{CE} = 7V$, $\beta = 100$

$R_2 = 5k$, $R_E = 500\Omega$

$$V_{cc} - 2I_c (R_c + R_E) S \times 0.07 I_{co} < \frac{1}{\alpha}$$

$I_{co} = 1nA$.

we have to find

S, I_c.

$$S = 1+\beta \times \frac{1 + \frac{R_B}{R_E}}{(1+\beta) + \frac{R_B}{R_E}}$$

$R_B = 100k \| 5K$

$R_B = \frac{100K \times 5K}{100K + 5K}$

$R_B = 4762\Omega$

$$S = (1+100) \times \frac{1 + \frac{4762\Omega}{500\Omega}}{(1+100) + \left(\frac{4762}{500}\right)}$$

$$\boxed{S = 9.617}$$

Applying KVL,

$$V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0$$

$$V_{cc} = I_c R_c + V_{CE} + (I_c + I_B) R_E$$

$$= I_c R_c + V_{CE} + (\beta I_B + I_B) R_E$$

$$V_{cc} = I_c R_c + V_{CE} + (\beta+1) I_B R_E$$

$$V_{cc} - V_{CE} = \beta I_B R_c + (\beta+1) I_B R_E$$

$$V_{cc} - V_{CE} = I_B (\beta R_c + (\beta+1) R_E)$$

$$I_B (\beta R_c + (\beta+1) R_E) = V_{cc} - V_{CE}$$

$$I_\beta = \frac{V_{cc} - V_{CE}}{\beta R_c + (\beta+1) R_E}$$

$$I_B = \frac{12 - 7}{100 \times 2k + (1+100) \times 500\Omega}$$

$$I_B = 20\mu A.$$

$$I_C = \beta I_B$$

$$I_C = 100 \times 20 \times 10^{-6}$$

$$I_C = 2 \times 10^{-3}$$

$$\boxed{I_C = 2mA.}$$

$$\left[V_{CC} - 2 I_C (R_C + R_E)\right](S)(0.07 I_{CO}) < \frac{1}{\theta}$$

$$\left[12 - 2 \times 2 \times 10^{-3} (2 \times 10^{3} + 500)\right](9.617) \times 0.07 \times 1 \times 10^{-9} < \frac{1}{\theta}.$$

$$1.346 \times 10^{-9} < \frac{1}{\theta}.$$

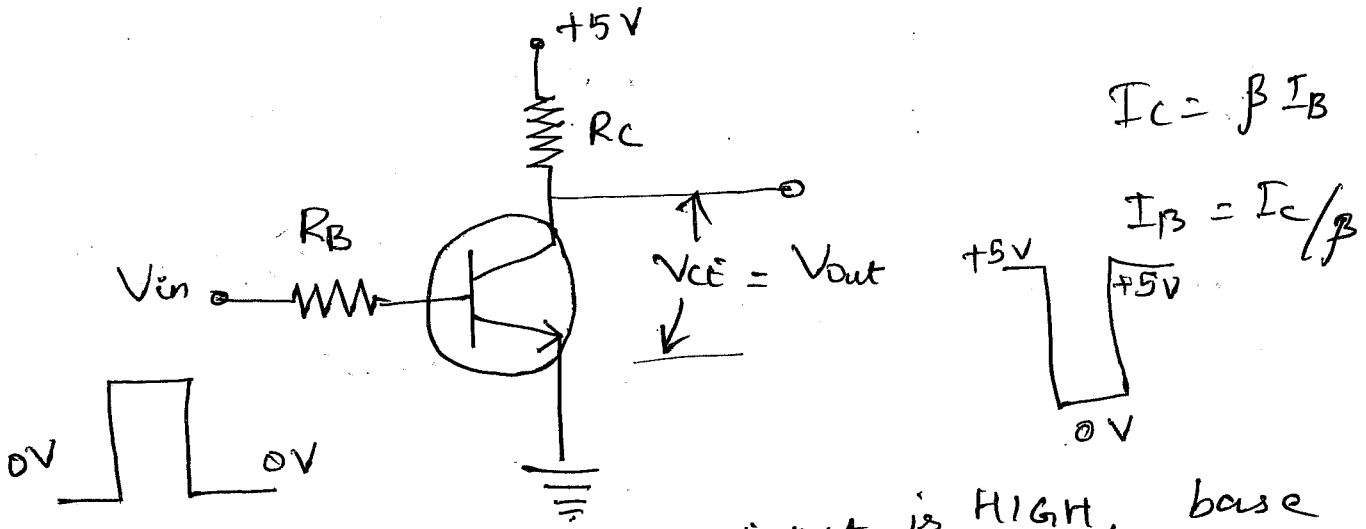
$$\theta < 7.427 \times 10^{8} \ ^\circ C/W$$

to make the circuit stable.

BIASING BJT SWITCHING CIRCUITS

Transistors are widely used in digital logic circuits as switching applications. In these applications the voltage levels periodically change between 'low' and 'High' voltage such as 0 V and +5 V.

In switching applications the transistor operates either cut off region or saturation region.

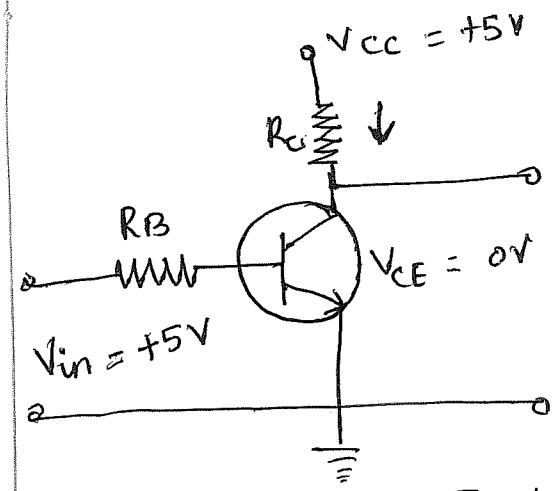


$I_C = \beta I_B$

$I_B = I_C/\beta$

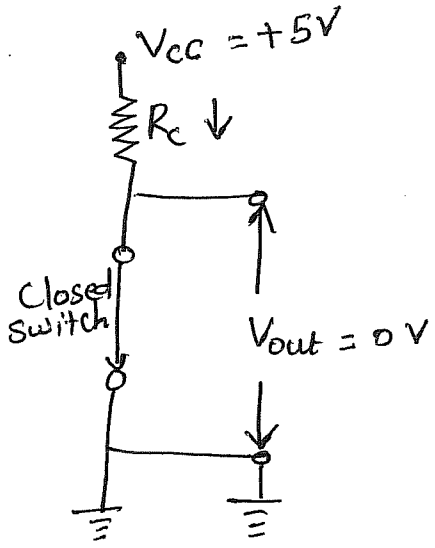
In this circuit when input is HIGH, base current flows and it is greater than I_C/β hence transistor is operated in saturated region. In saturation condition Voltage between collector and emitter $V_{CE(sat)}$ is 0.2 V to 0.3V and because of this transistor acts as closed switch. Consider Vcc is the supply voltage, R_C is the collector resistor, R_B is the base resistor the condition for closed switch and the condition for open switch can be explained as the following circuits.

Transistor Saturated



Transistor Saturated

≡



Switch ON
(Closed position)

* When the i/p is low base current and Collector current is zero and hence the transistor is operated in cut off. In cut off

$V_{CE} = V_{CC}$.

Hence transistor operate into saturation and cut off.

* In CB config $\frac{I_C}{I_E} = 1$ hence requires high i/p current (I_E)
* The CE → Configuration is prefered for switch
* In case of CC, Voltage gain is less than 1 hence requires high base voltage for forward bias.

That is the reason CE is used for switching circuits.

JFET Biasing Circuits

Like BJT the parameters of FET are also temperature dependent. The three terminals are Source, Gate and Drain. As temperature increases the drain resistance increases. So the drain current decreases. The DC analysis of FET are,

$$I_G = 0\ A$$

$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Unlike BJT the thermal runaway is not there in FET.

Biasing Circuits of JFET.

The different biasing circuits of FET are

1. Fixed Bias Circuit.
2. Self Bias Circuit
3. Voltage diver bias

1. Fixed bias circuit

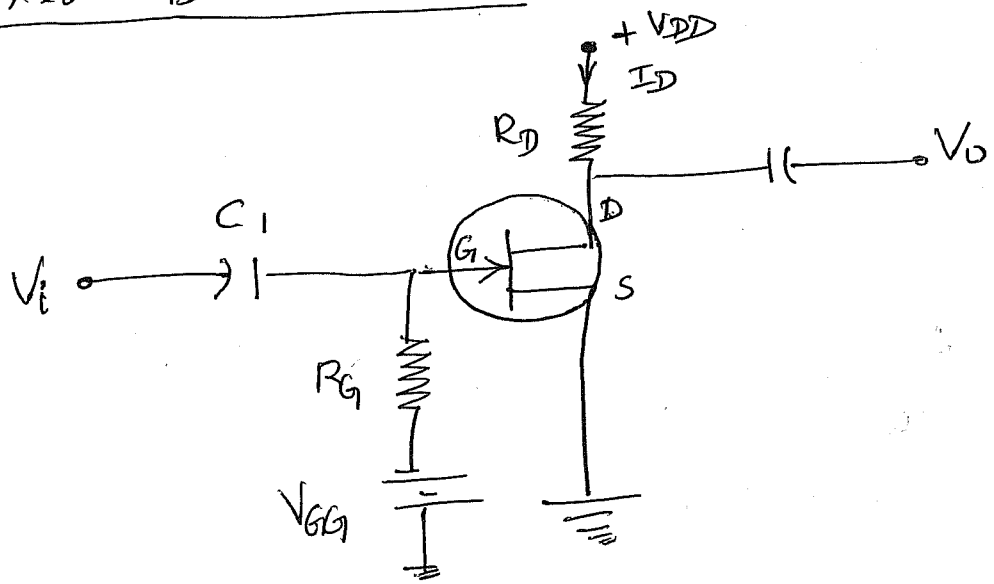
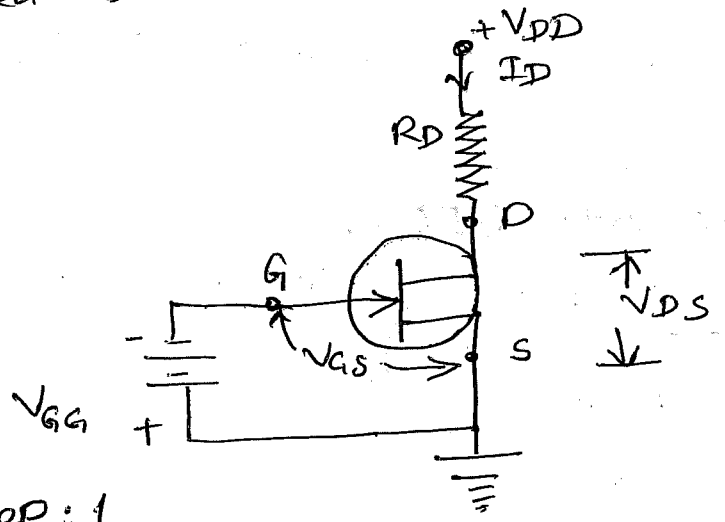


Figure shows the fixed bias Circuit for the n channel JFET. This is the simplest biasing arrangement. To make the gate source junction reverse biased, a separate voltage V_{GG} is connected such that gate is more negative than source.

For the dc analysis coupling capacitors are open circuits. The current through R_G is I_G, which is zero. This permits R_G to replace by short circuit equi... and the simplified fixed bias is as follows,



Step : 1

Calculate V_{GS}

To know for dc analysis $I_G = 0$ A and applying KVL to the input Circuit,

$$V_{GG} + V_{GS} = 0$$

$$\boxed{V_{GS} = -V_{GG}}$$

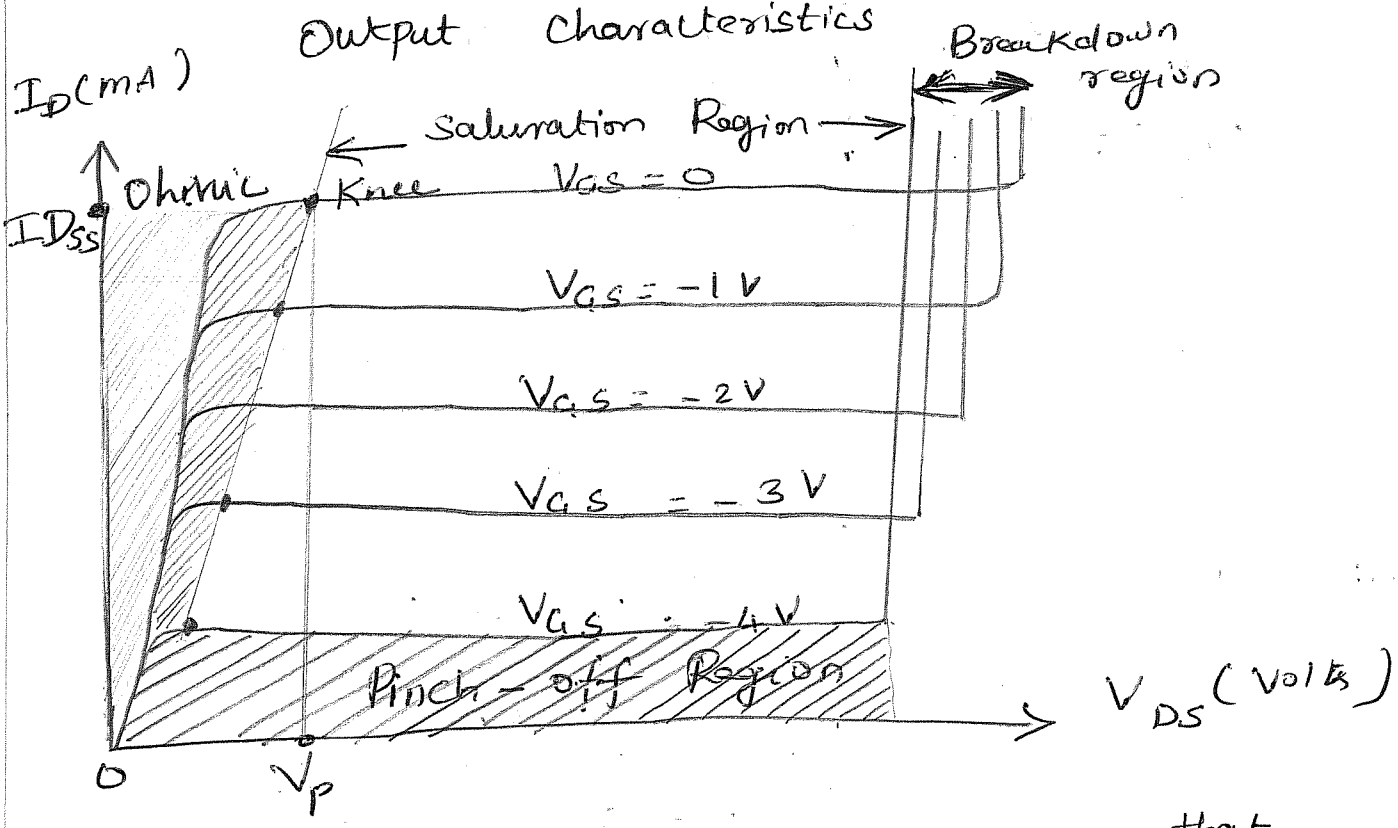
Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, hence the name fixed bias circuit.

Step: 2

Calculate I_{DQ}

The drain current I_D can be calculated using the following eqn,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$



Step: 3

I_D is choosen in such a way that for V_{DS} is negative for P Channel. V_{DS} is Positive for n Channel.

Calculate V_{DS}

The drain to source voltage of drain circuit can be determined by applying KVL,

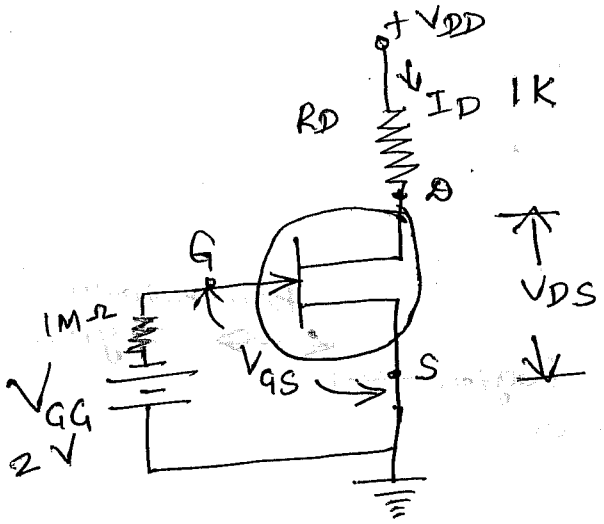
$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

The main drawback of fixed bias circuit of FET is it requires two power supplies.

For the circuit shown in fig. Calculate

a) V_{GSQ}, b) I_{DQ}, c) V_{DSQ} d) V_D



(i) $V_{GSQ} = -V_{GG}$ $\quad \because I_G = 0, \; I_G R_G = 0$

$V_{GSQ} = -2V$

(ii) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10 \times 10^{-3}\left(1 - \left(\frac{-2}{-4}\right)\right)^2$

$= 10 \times 10^{-3}(1 - 0.5)^2 = 10 \times 10^{-3} \times 0.5^2$

$\boxed{I_D = 2.5\,mA}$

$V_{DSQ} = V_{DD} - I_D R_D$

$= 8V - 2.5mA \times 1K$

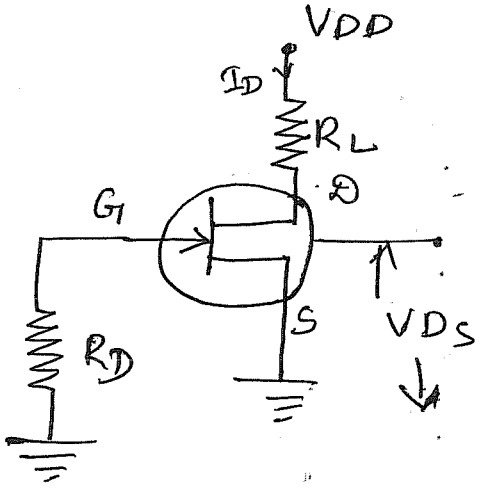
$= 8 - 2.5 \times 10^{-3} \times 1 \times 10^3$

$V_{DSQ} = 5.5\,V.$

$V_D = V_{DS} + V_S = 5.5 + 0$

$V_D = 5.5\,V$

DC Load Line and Bias Point



$$V_{DD} - I_D R_L - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_L$$

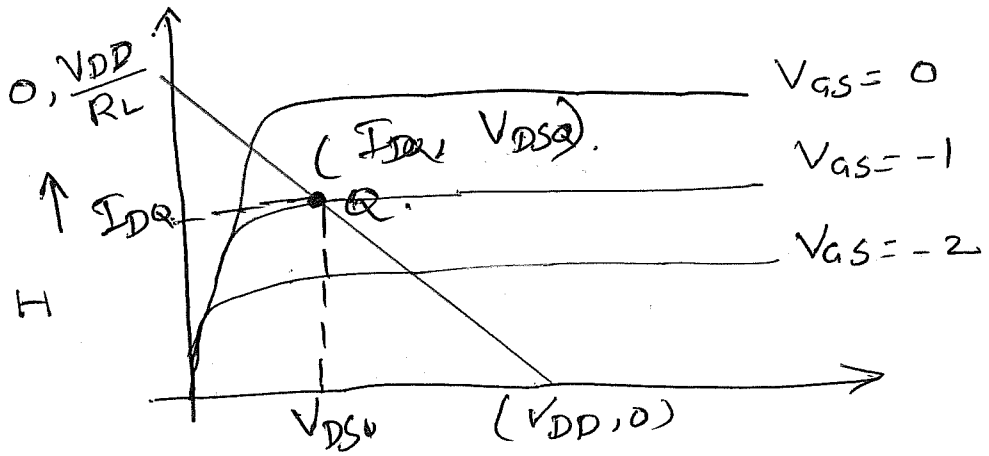
when $I_D = 0$,

$$V_{DD} = V_{DS}$$

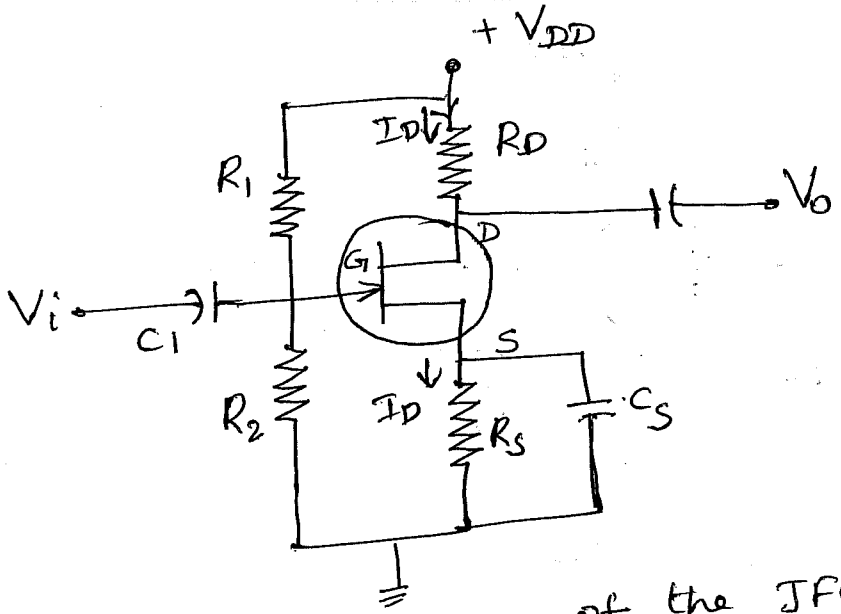
When

$$V_{DS} = 0, \quad I_D = \frac{V_{DD}}{R_L}$$

These are two end points of DC load line. The point at which dc load line intersects with the drain characteristics for a given V_{DS} is known as operating point Q. Once Q is known the quiescent Voltage V_{DS} and Quiescent Current I_D can be determined.



VOLTAGE DIVIDER BIAS CIRCUIT



Voltage at the Source of the JFET must be more positive than the voltage at the gate in order to keep the gate Source junction reverse biased.

The Source Voltage is,

$$V_S = I_D R_S$$

The gate Voltage is set by Resistors R_1 & R_2 Coupling capacitors C_1 & C_2 and source bypass Capacitor C_S are assumed to be open circuited

DC ANALYSIS

Step : 1

Calculate V_G

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

Step : 2

Obtain the expression for V_{GS}

Applying KVL to the input circuit

$$V_G - V_{GS} - I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

Step:3

Calculate I_{DQ}

I_{DQ} can be calculated using the equation,

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

step:4

Calculate V_{DS} and V_{GS}

Applying KVL to the output Circuit,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

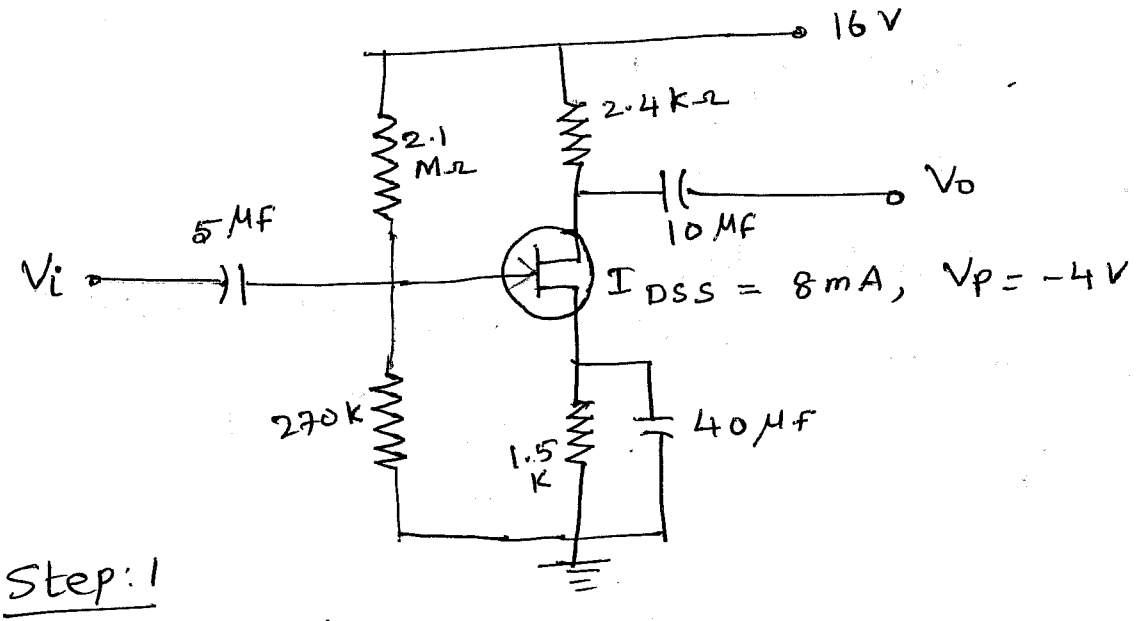
The 'Q' Point or Operating Point of JFET amplifier using Voltage divider bias is given by

Q Point = (I_{DQ}, V_{DSQ}) JFET

Q Point (I_{CQ}, V_{CEQ}) BJT

$$\boxed{\begin{aligned} I_{DQ} &= I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \\ V_{DSQ} &= V_{DD} - I_D(R_D + R_S) \\ V_{GS} &= V_G - I_D R_S \end{aligned}}$$

Pb Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} for the network.



Step: 1

Calculate V_G

$R_1 = 2.1\ M\Omega$, $V_{DD} = 16V$

$R_2 = 1.5\ K$

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$= \frac{16 \times 1.5K}{2.1M\Omega + 1.5K}$$

$$V_G = \frac{16 \times 1.5 \times 10^3}{2.1 \times 10^6 + 1.5 \times 10^3}$$

$$\boxed{V_G = 1.823\ V}$$

Step: 2

Obtain the expression for V_{GS}, Apply KVL to input,

$V_G = 1.823\ V$

$R_S = 1.5K$

$I_D = ?$

$$V_G - V_{GS} - I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = 1.823 - I_D \times 1.5 \times 10^3$$

$$V_{GS} = 1.823 - 1.5 \times 10^3 \times I_D$$

Step: 5 Calculate I_D

$V_{GS} = 1.823 - 1.5 \times 10^3 I_D$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$ $\quad 2\ I_{DSS} = 8\ mA,\ V_p = -4$

$I_D = 8\times10^{-3}\left[1 - \frac{(1.823 - 1.5\times10^3 \times I_D)}{-4}\right]^2$

$= 8\times10^{-3}\left[\left(1 - \frac{1.823}{-4} + \frac{1.5\times10^{+3} \times I_D}{-4}\right)\right]^2$

$= 8\times10^{-3}\left[1 + \frac{1.823}{4} - \frac{1500\ I_D}{4}\right]^2$

$I_D = 8\times10^{-3}\left[1.455 - 375\ I_D\right]^2$

$= 8\times10^{-3}\left[1.455^2 - 2\times1.455\times375\ I_D + (375\ I_D)^2\right]$

$= 1.455^2 \times 8\times10^{-3} - 2\times1.455\times375\times I_D\times8\times10^{-3} + 8\times10^{-3}\times375^2\ I_D^2$

$I_D = 16.936\times10^{-3} - 8.730\ I_D + 140625\times10^{-3}\times8\ I_D^2$

$I_D = 16.936\times10^{-3} - 8.730\ I_D + 1125\ I_D^2$

$I_D = 1125\ I_D^2 - 8.730\ I_D + 16.936\times10^{-3}$

$0 = 1125\ I_D^2 - 8.730\ I_D - I_D + 16.936\times10^{-3}$

$0 = 1125\ I_D^2 - 9.73\ I_D + 16.936\times10^{-3}$ $\quad a = 1125,\ b = -9.73,\ c = 16.93\times10^{-3}$

$I_D = \frac{-(-9.37) \pm \sqrt{(-9.73)^2 - 4\times1125\times16.93\times10^{-3}}}{2\times1125}$

$= \frac{9.37 \pm \sqrt{94.6729 - 76.185}}{2250}$

$= \frac{9.37 \pm 4.299}{2250}$

$$\frac{9.73 + 4.299}{2250} \quad \text{or} \quad \frac{9.73 - 4.299}{2250}$$

$6.237\ mA$ or $2.417\ mA$.

I_D is taken as 2.417. If 6.237 is considered the value of V_{DS} is negative. So that the minimum value 2.417 will be the I_D value.

$$\boxed{I_D = 2.417\ mA}$$

Step: 4

Calculate V_{DS}, V_{GS}, V_S, V_D and V_{DG}

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 16 - 2.417 \times 10^{-3}(2.4K + 1.5K)$$
$$= 16 - 2.417 \times 10^{-3}(2.4 \times 10^3 + 1.5 \times 10^3)$$
$$= 16 - 2.417 \times 10^{-3} \times 10^3 (2.4 + 1.5)$$

$$\boxed{V_{DS} = 6.5737\ V}$$

$$V_{GS} = 1.823 - I_D R_S$$
$$= 1.823 - (2.417 \times 10^{-3} \times 1.5 \times 10^3)$$
$$= 1.823 - (2.417 \times 1.5)$$
$$= 1.823 - 3.6255$$
$$V_{GS} = -1.8025\ V$$

$$V_S = I_D R_S$$
$$= 2.417 \times 10^{-3} \times 1.5 \times 10^3$$

$$\boxed{V_S = 3.6255\ V}$$

$V_D = V_{DD} - I_D R_D$

$= 16 - (2.417 \times 10^{-3} \times 2.4 \times 10^{3})$

$V_D = 16 - (2.417 \times 2.4)$

$\boxed{V_D = 10.2\ V}$

$V_{DG} = V_D - V_G$

$= 10.2 - 1.823$

$\boxed{V_{DG} = 8.377}$

Ans

(i) $V_G = 1.823\ V$

(ii) $I_D = 2.417\ mA$

(iii) $V_{DS} = 6.5737\ V$

(iv) $V_{GS} = -1.8025\ V$

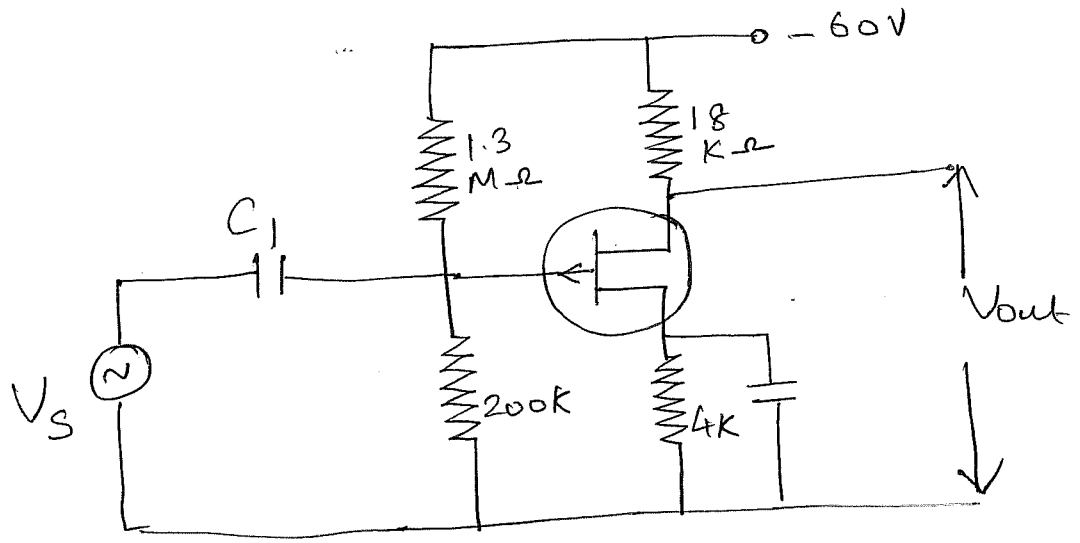
(v) $V_S = 3.6255\ V$

(vi) $V_D = 10.2\ V$

(vii) $V_{DG} = 8.377\ V$

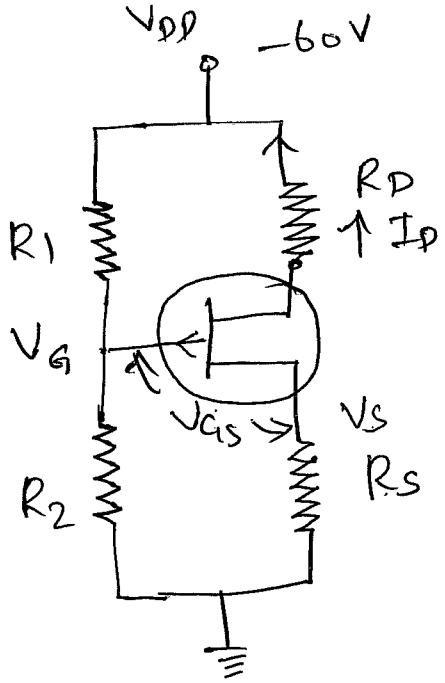
(b) For the Circuit shown in figure, the FET has $V_p = 4\ V$, $I_{DSS} = 4\ mA$.

Calculate (i) I_{DSQ} (ii) V_{GSQ} (iii) V_{DSQ}.



Soln

The simplified Circuit for dc analysis is shown as,



$R_S = 4\,K$
$R_D = 18\,K$
$R_1 = 1.3\,M\Omega$
$R_2 = 200\,K\Omega$
$V_{DD} = -60\,V$

Step: 1

Calculate V_G

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

$$= \frac{200 \times 10^{+3}}{1.3 \times 10^{6} + 200 \times 10^{3}} \times (-60)$$

$$\boxed{V_G = -8\,V}$$

Step: 2

Obtain the expression for V_{GS}

Apply KVL to the input Circuit,

$V_S = -I_D R_S$ for P-Chanel JFET

$$V_G - V_{GS} - V_S = 0$$

$$V_G - V_{GS} - (-I_D R_S) = 0$$

$$V_G - V_{GS} + I_D R_S = 0$$

$$V_{GS} = V_G + I_D R_S$$

$$V_{GS} = -8 + I_D R_S$$

$I_{DSS} = 4\,mA$

$V_{GS} = -8 + I_D R_S$

$V_p = 4V$

$R_S = 4 \times 10^3$

Step:3 Calculate I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$I_D = 4\times10^{-3}\left[1 - \frac{(-8 + I_D R_S)}{4}\right]^2$$

$$= 4\times10^{-3}\left[1 + \frac{8}{4} - \frac{I_D R_S}{4}\right]^2$$

$$= 4\times10^{-3}\left[1 + 2 - \frac{I_D \times 4\times10^3}{4}\right]^2$$

$$I_D = 4\times10^{-3}\left[3 - 1000 I_D\right]^2$$

$$I_D = 4\times10^{-3}\left[3^2 - 2\times3\times1000 I_D + 1000^2 I_D^2\right]$$

$$I_D = 4\times10^{-3}\times9 - 2\times3\times1000 I_D \times 4\times10^{-3} + 4\times10^{-3}\times100^2 I_D^2$$

$$I_D = 36\times10^{-3} - 24 I_D + 4000 I_D^2$$

$$36\times10^{-3} - 24 I_D - I_D + 4000 I_D^2 = 0$$

$$4000 I_D^2 - 25 I_D + 36\times10^{-3} = 0$$

$a = 4000$

$b = -25$

$c = 36\times10^{-3}$

$$I_D = \frac{-(-25) \pm \sqrt{(-25)^2 - 4\times4000\times36\times10^{-3}}}{2\times4000}$$

$$I_D = \frac{25 \pm \sqrt{625 - 576}}{8000}$$

$$I_D = \frac{25 \pm \sqrt{49}}{8000} = \frac{25 \pm 7}{8000} = \frac{25+7}{8000} \text{ or } \frac{25-7}{8000}$$

$I_D = 2.25\,mA$ or $I_D = 4\,mA$.

We calculate V_{DS} using $I_D = 4\,mA$.

$$V_{DS} = V_{DD} - (-I_D(R_S + R_D))$$

$$= -60 + 4m\Omega\,(4K + 18K)$$

$$= -60 + 4\times10^{-3}\,(4\times10^3 + 18\times10^3)$$

$V_{DS} = -60 + 88 = 28\ V$

$V_{DS} = 28\ V$. For P channel FET V_{DS} is negative. Here V_{DS} is not negative. Hence the value of I_D chosen as 4mA is neglected. is invalid.

Step: 4

Calculate V_{DS} and V_{GS}

$$V_{DS} = V_{DD} - (-I_D(R_S + R_D))$$

$$= -60 - \left(-2.25 \times 10^{-3} (4 \times 10^3 + 18 \times 10^3)\right)$$

$$V_{DS} = -60 - 49.5$$

$$\boxed{V_{DS} = -10.5\ V}$$

$$\boxed{I_D = 2.25\ mA}$$

$$V_{GS} = -8 + I_D R_S$$

$$= -8 + 2.25 \times 10^{-3} (4 \times 10^3)$$

$$V_{GS} = -8 + 9 = 1\ V$$

Ans

$V_{DS} = -10.5\ V$

$V_{GS} = 1\ V$

$I_D = 2.25\ mA$

$V_G = -8\ V$

JFET

P channel $V_{DS} = V_{DD} - (-I_D(R_S + R_D))$

V_{DS} is always Negative

N channel. $V_{DS} = V_{DD} - I_D(R_S + R_D)$

V_{DS} is always positive

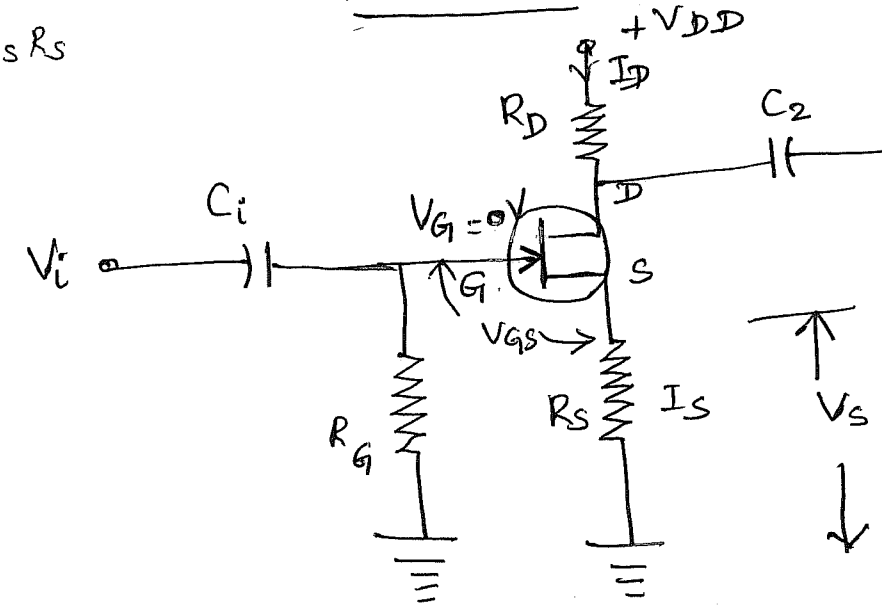
P → V_{DS} → −ve
N → V_{DS} → +ve

SELF BIAS CIRCUIT

Self bias Circuit is the most Common type of JFET Bias. JFET should be operated such that the gate source junction is always reverse biased. This condition requires a negative V_{GS} for an n channel JFET and a positive V_{GS} for p Channel JFET.

This can be achieved by self biasing arrangement. The gate resistor R_G does not affect the bias because it has no voltage drop across it. Therefore gate remains at 0V. R_G is used to isolate ac signal from ground. The voltage drop across resistor R_S makes the gate source junction reverse biased.

n Channel



$V_S = I_S R_S$

R_S makes Source Positive

$I_S = I_D$

$V_G = 0$

$V_S = I_S R_S$

$V_S = I_D R_S$

$V_S = I_D R_S$

$V_{GS} = V_G - V_S$

$= 0 - I_D R_S$

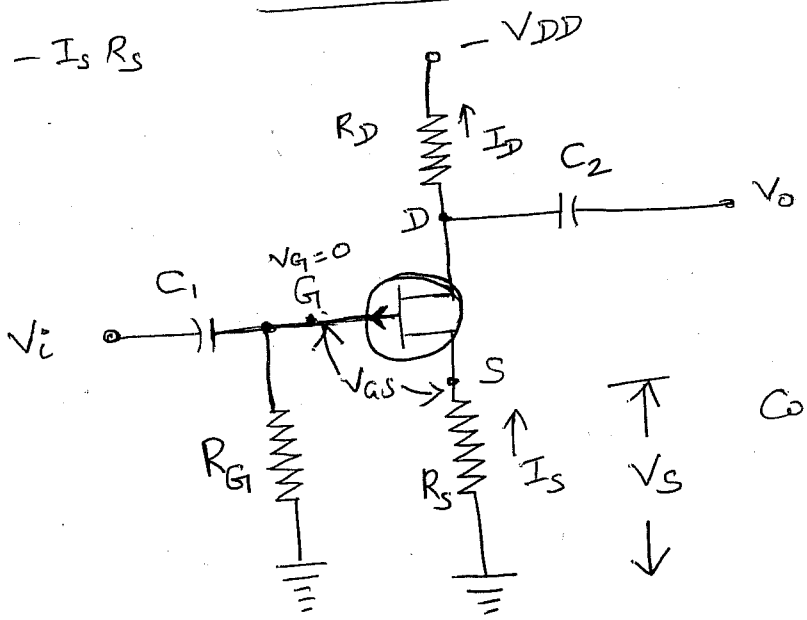
$$V_{GS} = -I_D R_S$$

$$I_S = I_D$$ in All JFETS

P Channel

$V_S = -I_S R_S$

R_S makes source negative



$V_{GS} = V_G - V_S$

$= 0 - (-I_S R_S)$

$V_{GS} = I_S R_S$

$\boxed{V_{GS} = I_D R_S}$

Coz $I_S = I_D$

DC Analysis

Step : 1 Obtain the expression for V_{GS}

For 'n' channel FET "I_S" produces a voltage drop across R_S and makes the source positive with respective to ground. Since $I_S = I_D$ and $V_G = 0$. We know that $V_G = 0$, so $V_S = I_S R_S$.

$V_S = I_S R_S \quad [V_G = 0]$

$V_S = I_D R_S \quad [I_S = I_D]$

$V_{GS} = V_G - V_S$

$= 0 - V_S$

$= 0 - I_D R_S$

V_{GS} = is negative

$\boxed{V_{GS} = -I_D R_S}$

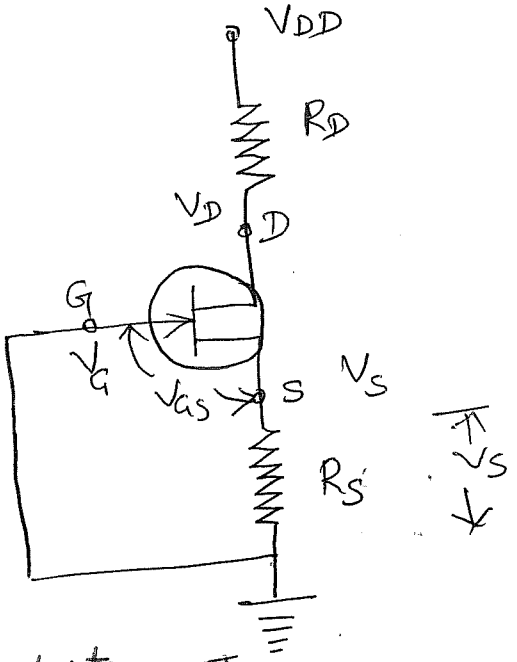
b) For p channel FET "I_S" produces a Voltage drop across R_S and makes the Soura negativ with respective to ground. Since $I_S = I_D$ and $V_G = 0$ then,

$$V_{GS} = V_G - V_S \qquad V_S = I_S R_S$$

$$V_{GS} = 0 - (I_D R_S)$$

$$\boxed{V_{GS} = -I_D R_S}$$

Circuit Diagram for DC Analysis [simplified]



$V_G = 0$ There is no source resistor R_G.

Step:2 Calculate I_{DQ}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Sub the value of V_{GS} in the above expression,

$$V_{GS} = -I_D R_S,$$

$$I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Step :3 Calculate V_{DS}

Applying KVL to the ouput Circuit,

$$V_{DD} - I_D R_D - V_{DS} - V_S = 0$$

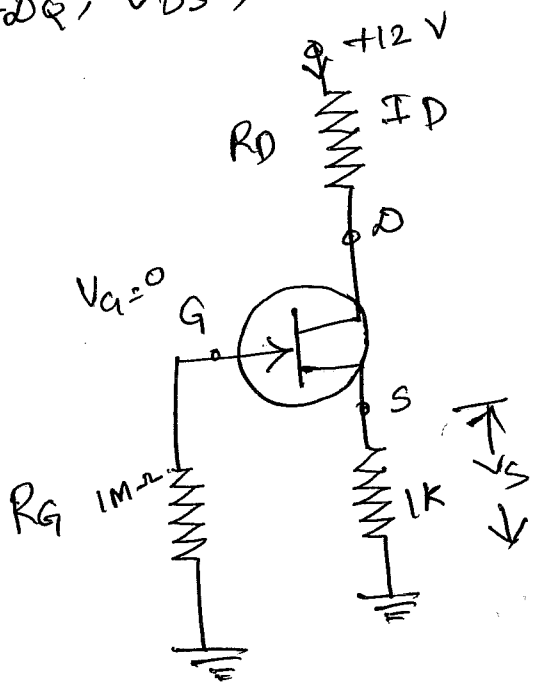
xly by (-), $V_S + V_{DS} + I_D R_D - V_{DD} = 0$.

$$V_{DS} = V_{DD} - V_S - I_D R_D$$

$$= V_{DD} - I_D R_S - I_D R_D$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

Pb For the Circuit shown in figure Calculate V_{GSQ}, I_{DQ}, V_{DS}, V_S and V_D.



$I_{DSS} = 8\,mA$

$V_P = -4V$

Step:1

Obtain the expression for V_{GS}

$$\boxed{V_{GS} = -I_D R_S}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = I_{DSS}\left[1 - \frac{(-I_D R_S)}{V_P}\right]^2$$

$$= I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2$$

$$= I_{DSS}\left[1 + \frac{I_D R_S}{-4}\right]$$

Step:2

Calculate I_D, V_{GS} and V_S

$$I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2$$

$$I_D = 8\times10^{-3}\left(1 + \frac{I_D \times 1\times10^{3}}{-4}\right)^2$$

$$= 8\times10^{-3}\left(1 - \frac{1000\, I_D}{4}\right)^2$$

$$= 8\times10^{-3}\left(1 - 250\, I_D\right)^2$$

$$= 8\times10^{-3}\left(1 - 2\times1\times250 I_D + (250\, I_D)^2\right)$$

$$= 8\times10^{-3}\left(1 - 500\, I_D + 62500\, I_D^2\right)$$

$$I_D = 8\times10^{-3} - 4\, I_D + 500\, I_D^2$$

$$500\, I_D^2 - 4\, I_D + 8\times10^{-3} - I_D = 0$$

$a = 500$
$b = -5$
$c = 8\times10^{-3}$

Solving quadratic eqn

$$0 = 500\, I_D^2 - 5\, I_D + 8\times10^{-3}$$

$$= \frac{-(-5) \pm \sqrt{(-5)^2 - 4\times500\times8\times10^{-3}}}{2\times500}$$

$$= \frac{+5 \pm \sqrt{25-16}}{1000} = \frac{-5 \pm \sqrt{9}}{1000}$$

$$= \frac{+5 \pm 3}{1000}$$ 8 mA or 2 mA. $\boxed{I_D = 2\text{mA}}$

$$I_D = \frac{+5+3}{1000} \text{ or } \frac{+5-3}{1000} \Rightarrow \frac{2}{1000} \text{ or } \frac{+8}{1000}.$$

2 mA or 8 mA.

I_D is Chosen as 2mA.

I_D Cannot have 8mA. Value because maximum Value of I_D, I_{DSS} is Consider $I_D = 2\text{mA}$.

$$V_{GSQ} = -I_D R_S$$

$$= -2\times10^{-3}\times1\times10^{3}$$

$$\boxed{V_{GS} = -2\text{ V}}$$

$V_S = I_D R_S$

$V_S = 2 \times 10^{-3} \times 1 \times 10^{3}$

$\boxed{V_S = 2V}$

Step:3 Calculate V_{DS}

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

$V_{DS} = 12 - 2 \times 10^{-3} (2.2 \times 10^{3} + 1 \times 10^{3})$

$= 12 - 2 \times 10^{-3} \times 3.2 \times 10^{3}$

$= 12 - 6.4$

$\boxed{V_{DS} = 5.6V}$

Step: 4 Calculate V_D

$V_D = V_{DS} + V_S$

$V_D = 5.6 + 2$

$\boxed{V_D = 7.6V}$

Ans

$I_D = 2mA$

$V_{GS} = -2V$

$V_S = 2V$

$V_{DS} = 5.6V$

$V_D = 7.6V$

Ph Calculate the value of feed back resistor (R_S) required to self bias as N channel JFET with $I_{DSS} = 40\ mA$, $V_p = -10$ and $V_{GSQ} = -5V$.

Soln

To find $R_S = ?$

Given

$I_{DSS} = 40mA$, $V_p = -10$, $V_{GS} = -5V$

Step: 1

Calculate I_D

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$= 40\left[1 - \left(\frac{-5}{-10}\right)\right]^2 = 40\left[1 + \left(\frac{-1}{2}\right)\right]^2$$

$$I_D = 40 \times (0.5)^2 \text{ mA}$$

$$I_D = 40 \times 10^{-3} \times [0.5]^2$$

$$\boxed{I_D = 10mA}$$

Step: 2 Calculate R_S

For self bias Circuit

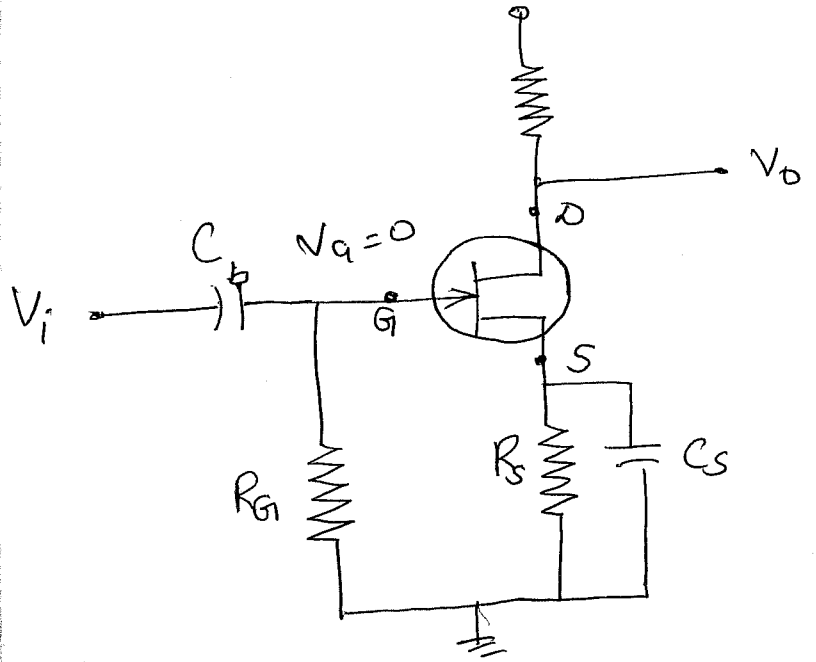
$$V_G = -I_D R_S \qquad V_{GQ} = -I_{DQ} R_S$$

$$R_S = \frac{-V_{GQ}}{-I_{DQ}} = \frac{-(-5)}{10\ mA} = 500\ \Omega$$

$$\text{(or)} = \frac{1}{2} \times 10^3 = 0.5 \times 10^3$$

$$\boxed{R_S = 500\ \Omega}$$

Pb $V_p = -2V$, $I_{DSS} = 1.65\ mA$. for the circuit in fig. It is desired to bias the circuit at $I_D = 0.8\ mA$. $V_{DD} = 24V$. Calculate (i) V_{GS} (ii) g_m (iii) R_S



Soln

Calculate V_{GS}

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$\frac{I_D}{I_{DSS}} = \left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_p}$$

$$1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_p} = 1 - \sqrt{\frac{I_D}{I_{DSS}}}$$

$$V_{GS} = V_p\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = -2\left[1 - \sqrt{\frac{0.8\times10^{-3}}{1.65\times10^{-3}}}\right]$$

$$\boxed{V_{GS} = -0.6074\ V}$$

Step: 2

Calculate g_m = ?

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_{mo} = \frac{-2I_{DSS}}{V_P}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

g_m → Transconductance of JFET

g_{mo} → maximum Trans conductance of FET.

$$g_{mo} = \frac{-2\times 1.65\,mA}{-2V} = 1.65\ msec$$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$= 1.65\times10^{-3}\left[1 - \frac{(-0.6074)}{(-2)}\right]$$

$$= 1.65\times10^{-3}\left[0.6963\right]$$

$$= 1.65\times10^{-3}\times 0.6963$$

$$\boxed{g_m = 1.15\ ms}$$

Step: 3

Calculate R_S

$$V_{GS} + I_D R_S = 0$$

$$I_D R_S = -V_{GS}$$

$$R_S = \frac{V_{GS}}{I_D}$$

$$R_S = -\frac{0.6074\ V}{0.8\ mA}$$

$$R_S = 759.25\ \Omega$$

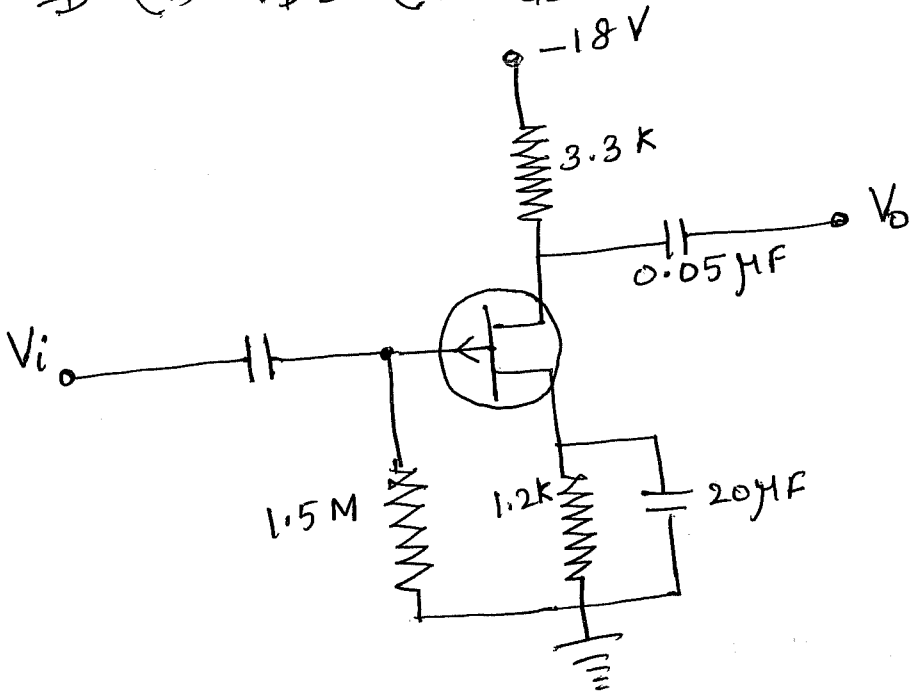
Ans

$V_{GS} = -0.6074\ V$

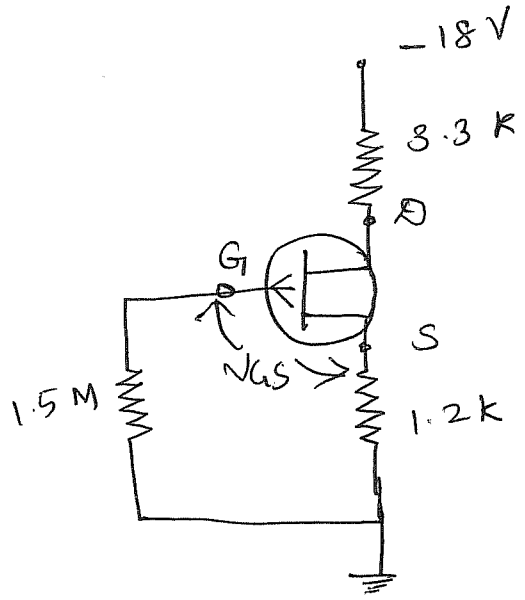
$g_m = 1.15\ mS$

$R_S = 759.25\ \Omega$

EX The FET shown in figure has $|I_{DSS}| = 12\ mA$ and $V_p = 5\ V$. Calculate the quiescent values of (i) I_D (ii) V_{DS} (iii) V_{GS}.



Soln



Step: 1

To obtain the value for V_{GS} Applying KVL to the input circuit,

$$V_{GS} - I_D R_S = 0$$

$$V_{GS} = I_D R_S$$

$I_{DSS} = 12\,mA$

$V_P = 5V$

$R_S = 1.2K$

$R_G = 1.5M$

$R_D = 3.3k$

$V_{DD} = -18V$

Step: 2

Calculate I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12\times10^{-3}\left(1 - \frac{1.2\times10^{3}\, I_D}{5}\right)^2$$

$$I_D = 12\times10^{-3}\left(1 - 240\, I_D\right)^2$$

$$I_D = 12\times10^{-3}\left(1^2 - 2\times1\times240\, I_D + 240^2\, I_D^2\right)$$

$$I_D = 12\times10^{-3} - 12\times10^{-3}\times2\times1\times240\, I_D + 240^2\, I_D^2 \times 12\times10^{-3}$$

$$I_D = 12\times10^{-3} - 5.76\, I_D + 691\, I_D^2$$

$$12\times10^{-3} - 5.76\, I_D - I_D + 691\, I_D^2 = 0$$

$691 I_D^2 - 6.76 I_D + 12 \times 10^{-3} = 0$

$a = 691$
$b = -6.76$
$C = 12 \times 10^{-3}$

$$I_D = \frac{-(-6.76) \pm \sqrt{(-6.76)^2 - (4 \times 691 \times 12 \times 10^{-3})}}{2 \times 691}$$

$$I_D = \frac{6.76 \pm \sqrt{45.6976 - 33.168}}{1382}$$

$$I_D = \frac{6.76 \pm \sqrt{12.5296}}{1383} = \frac{6.76 \pm 3.539}{1383}$$

$$I_D = \frac{6.76 + 3.53.}{1383} \text{ or } \frac{6.76 - 3.539}{1383}$$

$I_D = \ldots 0.00744$ or $\ldots 0.002325$

$I_D = 7.4 mA$ or $2.3 mA$.

Select $I_D = 2.33 mA$ for FET, V_{DS} should be negative.

$$I_D = 2.33 \text{ mA}$$

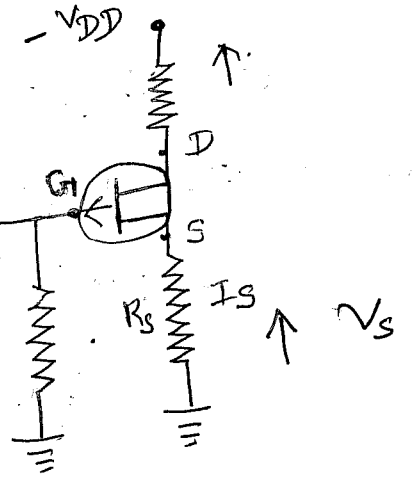
Step: 3

To calculate V_{DS} and V_{GS} Apply KVL to O/P Portion,

$V_{DS} = ?$

Apply KVL to the Output portion,

$I_S R_S + V_{DS} + I_D R_D + (+V_{DD}) = 0$



$$V_{DS} = V_{DD} - [-I_D(R_S + R_D)]$$

$$= -18 - [-2.33(1.2\times10^{3} + 3.3\times10^{3})]$$

$$= -18 + 10.485$$

$$V_{DS} = -7.515\ V$$

Ans

$I_D = 2.33\ mA$

$V_{DS} = -7.515$

$V_{GS} = 2.796\ V$

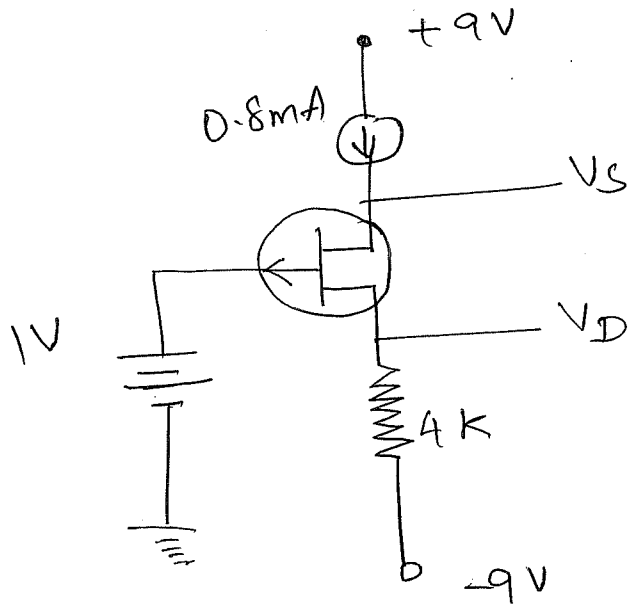
$V_{GS} = I_D R_S$

$V_{GS} = 2.33\times10^{-3} \times 1.2\times10^{3}$

$V_{GS} = 2.796\ V$

Ph Determine the quiescent Circuit Current and Voltage values of a P Channel JFET Circuit.

$I_{DSS} = 2.5\ mA$, $V_P = +2.5\ V$



$R_D = 4k$

$I_D = 0.8mA$

Soln

Given $I_D = 0.8\ mA$

$(-9) + I_D R_D = V_D$

$V_D = I_D R_D - 9V$

$V_D = I_D R_D - 9V$

$= 0.8\ mA \times 4\times10^{3} - 9$

$\boxed{V_D = -5.8\ V}$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\frac{0.8}{\times 10^{-3}} = \frac{2.5}{\times 10^{-3}}\left(1 - \frac{V_{GS}}{2.5}\right)^2 = 2.5\times10^{-3}\left(1 - 0.4\right)$$

$$\frac{0.8}{\times 10^{-3}} = \left(2.5 - V_{GS}\right)^2$$

$$0.8 = 6.25 - 2\times 2.5 \times V_{GS} + V_{GS}^2$$

$$= 6.25 - 5V_{GS} + V_{GS}^2$$

$$= V_{GS}^2 - 5V_{GS} - 0.8V_{GS} + 6.25$$

$$0.8 = V_{GS}^2 - 5.8V_{GS} + 6.25$$

$$\frac{-5.8 \pm \sqrt{(-5.8)^2 - 4\times 1\times 6.25}}{2\times 1}$$

$V_P = 2.5$

$I_D = 0.8\times10^{-3}$

$I_{DSS} = 2.5\times10^{-3}$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$0.8\times10^{-3} = 2.5\times10^{-3}\left(1 - \frac{V_{GS}}{2.5}\right)^2$$

$$0.8\times10^{-3} = 2.5\times10^{-3}\left(1 - 0.4\,V_{GS}\right)^2$$

$$= 2.5\times10^{-3}\left(1^2 - 2\times1\times0.4V_{GS} + 0.4^2V_{GS}^2\right)$$

$$= 2.5\times10^{-3}\left(1 - 0.8V_{GS} + 0.16V_{GS}^2\right)$$

$$= 2.5\times10^{-3} - 0.8\times2.5\times10^{-3}\times V_{GS} + 0.16\times2.5\times10^{-3}V_{GS}^2$$

$$= 2.5\times10^{-3} - 2\times10^{-3}\times V_{GS} + 0.4\times10^{-3}V_{GS}^2$$

$$0.8\times10^{-3} = 10^{-3}\left[2.5 - 2V_{GS} + 0.4V_{GS}^2\right]$$

$$0.8 = 2.5 - 2V_{GS} + 0.4V_{GS}^2$$

$$0.0 = 0.4V_{GS}^2 - 2V_{GS} + 2.5 - 0.8$$

$b = -2$
$c = 1.7$.

$$0 = 0.4 V_{GS}^2 - 2 V_{GS} + 1.7$$

$$V_{GS} = \frac{-(-2) \pm \sqrt{(-2)^2 - 4 \times 0.4 \times 1.7}}{2 \times 0.4}$$

$$V_{GS} = \frac{2 \pm \sqrt{4 - 2.72}}{0.8} \Rightarrow \frac{2 \pm 1.131}{0.8}$$

$\frac{2+1.131}{0.8}$ or $\frac{2-1.131}{0.8}$

P-2-10

doubt.

3.9 or 1.086

$$\boxed{V_{GS} = 1.086\ V}$$

V_S = Apply KVL

$V_S + V_{GS} - = 0$

$V_S = 1 - V_{GS}$

$V_S = 1 - 1.086$

$$\boxed{V_S = -0.086 V}$$

$$V_{SD} = V_S - V_D = -0.086 - (-5.8) = 5.71\ V$$

$V_{SD} = 5.71$

$V_p - V_{GS} = 2.5 - 1.086 =$

$V_p - V_{GS} = 1.41\ V$

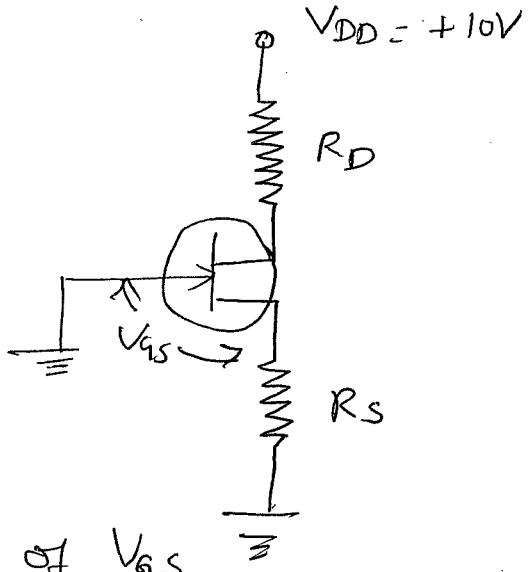
$$\boxed{V_{SD} > V_p - V_{GS}}$$, then we can say that the transistor is biased in the saturation region.

JFET Bias Circuit design

1. Design the bias voltage for the JFET Circuit shown in figure. JFET Parameters I_{DSS} = 8mA, I_{DSS} = 8mA, V_p = 4V. ASume I_D = 2mA, V_{DS} = 5V.

Soln

Asume JFET is biased in saturation region.



Step: 1

Calculation of V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\times 10^{-3} \quad 2 = 8\left(1 - \frac{V_{GS}}{(-4)}\right)^2$$

$$\times 10^{-3}\ 2 = (8 - 0.25)^2$$

$$\times 10^{-3}\ 2 = 8^2 - 2 \times 8 \times 0.25 V_{GS} + (0.25)^2 V_{GS}^2$$

$$\times 10^{-3}\ 2 = 16 - 4V_{GS} + 0.0625 V_{GS}^2$$

$$16 - 4V_{GS} - 2V_{GS} + 0.0625 V_{GS}^2 = 0$$

$$0.0625 V_{GS}^2 - 6 V_{GS} + 16 = 0$$

UNIT I - BIASING OF DISCRETE BJT, JFET AND MOSFET

(EC 8351)

POSSIBLE ASSESSMENT QUESTIONS

S.No	Questions	Blooms Level	CO'S
	PART A		
1.	What is operating point?	K1	CO 203.1
2.	What is thermal runaway?	K1	CO 203.1
3.	What is the impact of temperature on drain current of MOSFET?	K1	CO 203.1
4.	List the methods of biasing a JFET.	K1	CO 203.1
5.	Why is the operating point selected at the center of the active region?	K1	CO 203.1
6.	Define stability factor.	K1	CO 203.1
7.	List out the importance of selecting the proper operating point.	K1	CO 203.1
8.	Show a dc load line of the BJT	K2	CO 203.1
9.	Define the term biasing	K1	CO 203.1
10.	What are the operating region of N-channel MOSFET and how identify the operating region?	K1	CO 203.1
11.	List out the three stability factor	K1	CO 203.1
12.	What do you mean by punch through?	K1	CO 203.1
13.	Calculate the value of feedback resistor (R_e) required to self bias an N-channel JFET with I_{DSS} = 40 mA, V_p = -10 V and V_{GSQ} = -5V	K3	CO 203.1
14.	How can collector current be stabilized with respect to I_{ce} variations?	K1	CO 203.1
15.	Quote the stability factor S for a fixed circuit.	K1	CO 203.1
16.	Show the single stage self-biased circuit using PNP transistor.	K2	CO 203.1
17.	What is the need for biasing in transistor amplifier?	K1	CO 203.1
18.	Compare bias stabilization and compensation techniques.	K4	CO 203.1
19.	Why is temperature compensation required?	K1	CO 203.1
20.	List the conditions of thermal stability.	K1	CO 203.1
	PART B		
1.	i) Solve Emitter bias for BJT with I_e = 2mA, V_{cc}=18V ,V_{CE} = 10 V and β =150	K3	CO 203.1

	ii) Examine the stability factor of Self bias circuit of BJT.		
2.	i) Why biasing is necessary in BJT amplifier? ii)How will you select the operating point iii)Explain the concept of DC & AC load line with neat diagram. iv)Explain it using CE amplifier characteristics?	K2	CO 203.1
3.	Explain in detail the various types of bias compensation circuits with neat illustration	K5	CO 203.1
4.	Compare the various methods of biasing using BJT in term of their stability factor	K4	CO 203.1
5.	Analyze a BJT with a voltage divider bias circuit, and determine the change in the Q-point with a variation in β when the circuit contains an emitter resistor. Let the biasing resistors be R_{B1} =56kΩ,R_{B2}=12.2 kΩ,R_C =0.4 kΩ,V_{CC} =10V,$V_{BE(ON)}$ =0.7 V and β =100	K4	CO 203.1
6.	Determine the stability factors for voltage divider bias circuit and give reason why it is advantageous than fixed bias circuit.	K5	CO 203.1
7.	Explain with neat diagram and explain the source and drain resistance MOSFET	K5	CO 203.1
	PART C		
1.	Explain about common source self bias and voltage divider bias for FET ?	K5	CO 203.1
2.	Explain in detail about various methods of biasing MOSFET ?	K5	CO 203.1
3.	Explain with neat circuit diagram about Voltage Divider Bias method in BJT and derive the expressions for stability factor ?	K5	CO 203.1