

ARM Architecture

ARM Architecture Versions

- ARM means Advanced RISC Machines. ARM machines have a 32-bit Reduced Instruction Set Computer (RISC) Load Store Architecture. It is first RISC microprocessor for commercial use and market-leader for low-power and cost-sensitive embedded applications.
- The processor originated in England in 1984. At its inception ARM stood for Acorn RISC Machine. The first ARM reliant systems include the Acorn : BBC Micro, Masters and the Archimedes. During this early period they were used mostly for British educational systems and therefore, were not widely available or known outside England. However in 1987 the ARM became the first commercial RISC processor.
- The ARM is a Von Neumann, load/store architecture i.e. only 32-bit data bus for both instruction and data. Also for the load/store instruction access memory.
- Licenses ARM core designs to semiconductor partners who fabricate and sell to their customers. ARM does not fabricate silicon itself.
- First models had only a 26-bit program counter, limiting the memory space to 64 MB.
- In 1990, the research section of Acorn separated from the parent company and formed : Advanced RISC Machines Limited.
- The ARM is a 32-bit architecture. When used in relation to the ARM :
 1. Byte means 8 bits
 2. Halfword means 16 bits.
 3. Word means 32 bits.
- Most ARM's implement two instruction sets
 1. 32-bit ARM Instruction Set
 2. 16-bit Thumb Instruction Set

- Memory is addressed as a 32 bit address space. Data type can be 8 bit bytes, 16 bit half-words or 32 bit words and may be seen as a byte line folded into 4-byte words.
- ARM1 processor was the first commercialized RiSC processor and it contained 25,000 transistors.

ARM processor	Features
ARM1	<ul style="list-style-type: none"> • First version of ARM processor. • 26-bit addressing, no multiply / coprocessor.
ARM2	<ul style="list-style-type: none"> • ARM2, First commercial chip. • Included 32-bit result multiply instructions/coprocessor support.
ARM2a	<ul style="list-style-type: none"> • ARM3 chip with on-chip cache. • Added load and store. • Cache management.
ARM3	<ul style="list-style-type: none"> • ARM6, 32 bit addressing, virtual. • Memory support.
ARM7	<ul style="list-style-type: none"> • Most popular used today. • Suitable for DSP work.
ARM8	<ul style="list-style-type: none"> • It Includes a five stage pipeline. • Speculative instruction fetcher. • Processor to allow a higher clock speed.
ARM9	<ul style="list-style-type: none"> • Uses five stage pipeline. • Support Harvard Architecture chip.

ARM Features

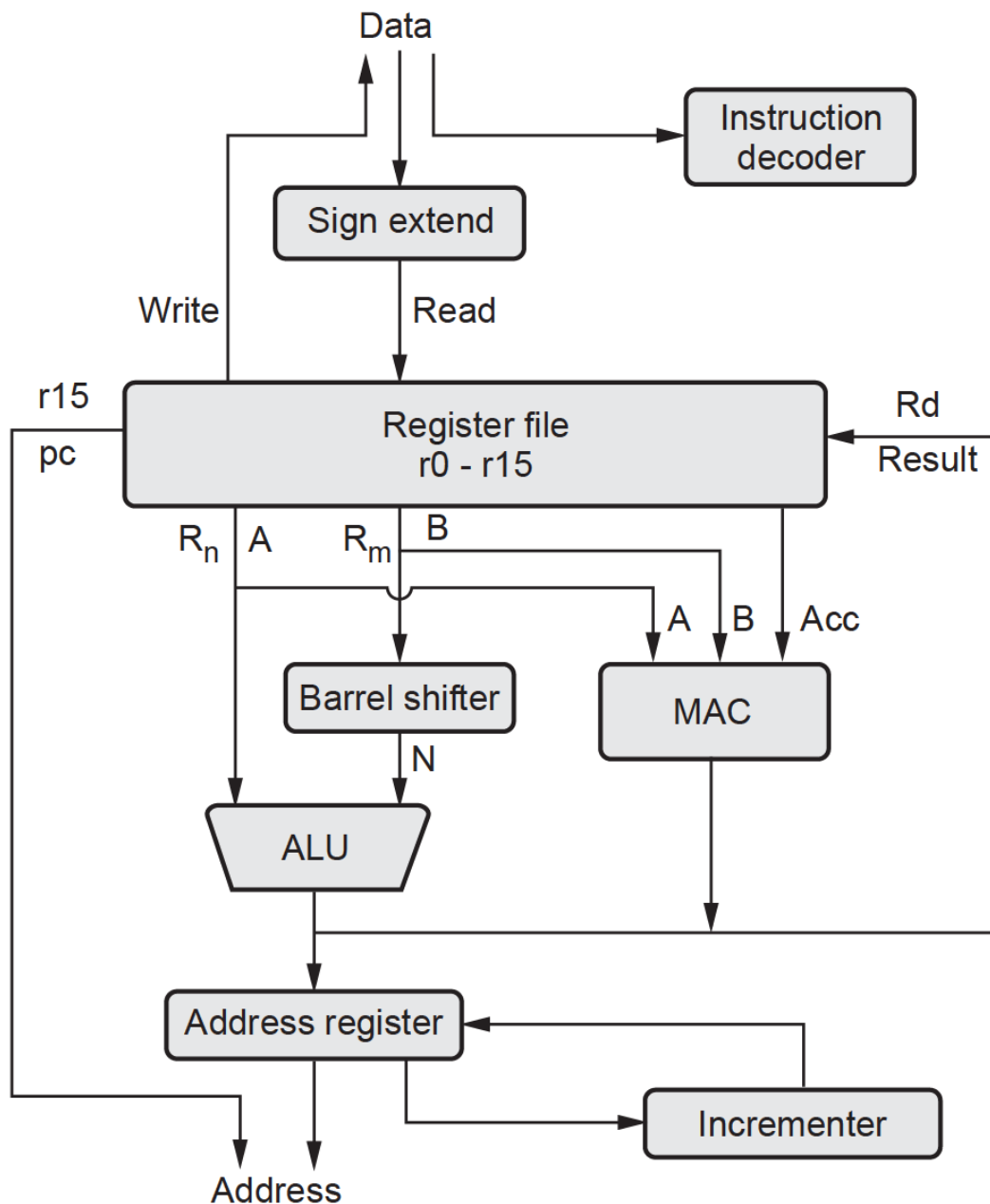
1. Thumb Set designed for 16-bit word lengths and instructions, which internally executes by same 32-bit core.
2. ARM views memory as a linear collection of bytes numbered upwards from zero. it contains memory management unit and memory protection unit.

3. Most operations are executed over registers.
4. All instructions can be conditional.
5. it uses Big-endian and Little-endian method.
6. The ARM processor supports 25 different instruction.
7. ARM provides no explicit return instruction.
8. The Software Interrupt (SWI) instruction is the only way an ARM processor can access resources controlled by the operating system.
9. Many Thumb data processing instructions use a 2-address format.
10. Jazelle Instruction Set : Introduces technological infrastructure for running Java code.
11. The ARM architecture has a large variety of addressing modes

ARM Architecture

- The ARM architecture processor is an advanced reduced instruction set computing [RISC] machine and it's a 32 bit RISC microcontroller.
- The ARM cortex is a complicated microcontroller within the ARM family that has ARMv7 design. There are 3 subfamilies within the ARM cortex family:
 - a) ARM Cortex Ax-series
 - b) ARM Cortex Rx-series
 - c) ARM Cortex Mx-series
- The ARM Architecture consists of following:
 - a) Arithmetic Logic Unit
 - b) Booth multiplier
 - c) Barrel shifter
 - d) Control unit
 - e) Register file

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- The ARM processor conjointly has other components like the Program status register, which contains the processor flags (Z, S, V and C).
- The modes bits conjointly exist within the program standing register, in addition to the interrupt and quick interrupt disable bits; Some special registers: Some registers are used like the instruction, memory data read and write registers and memory address register.

1. Priority encoder : The encoder is used in the multiple load and store instruction to point which register within the register file to be loaded or kept.
2. Multiplexers : Several multiplexers are accustomed to the management operation of the processor buses.
3. Arithmetic Logic Unit (ALU) : The ALU has two 32-bits inputs. The primary comes from the register file, whereas the other comes from the shifter. Status registers flags modified by the ALU outputs. The V-bit output goes to the V flag as well as the Count goes to the C flag. Whereas the foremost significant bit really represents the S flag, the ALU output operation is done by NORed to get the Z flag. The ALU has a 4-bit function bus that permits up to 16 opcode to be implemented.
4. Booth multiplier factor : The multiplier factor has 3 32-bit inputs and the inputs return from the register file. The multiplier output is barely 32-Least Significant Bits of the merchandise. The entity representation of the multiplier factor is shown in the above block diagram. The multiplication starts whenever the beginning 04 input goes active. Fin of the output goes high when finishing.
5. Barrel shifter : The barrel shifter features a 32-bit input to be shifted. This input is coming back from the register file or it might be immediate data. The shifter has different control inputs coming back from the instruction register. The Shift field within the instruction controls the operation of the barrel shifter. This field indicates the kind of shift to be performed. The quantity by which the register thought to be shifted is contained in an immediate field within the instruction or it might be the lower 6 bits of a register within the register file.
6. Control unit : The control unit is sometimes a pure combinational circuit design. Here, the control unit is implemented by easy state machine. The processor timing is additionally included within the control unit. Signals

from the control unit are connected to each component within the processor to supervise its operation.

7. Incremented :

- For load and store instructions, the incremented updates the contents of the address register before the processor core reads or writes the next register value from or to the consecutive memory location.
- The processor core continues the execution of instruction. Only when an exception or interrupt occurs, the normal execution flow is changed.

8. Address Register : This holds the address generated by the load and store instructions and places it on the address bus.

9. Instruction decoder : It decodes the instruction opcode read from the memory and then the instruction is executed.

10. Register file : This is a bank of 32-bit registers used for storing data items.

