DC Load Line and Bias Point – DC analysis of Transistor circuits

Biasing is the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). The operating point of a device, also known as bias point, quiescent point, or Q-point, is the point on the output characteristics that shows the DC collector–emitter voltage (V_{ce}) and the collector current (I_c) with no input signal applied shown in figure 1.3.1.

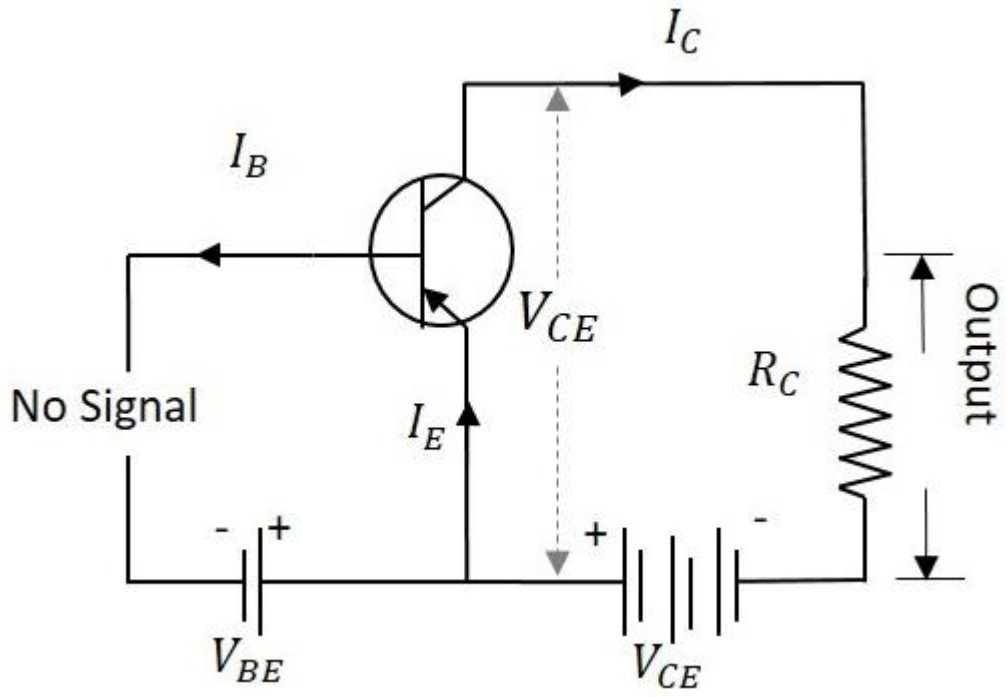


Figure 1.3.4 DC condition to draw dc load line

Diagram Source Brain Kart

We can draw a straight line on the graph of I_C versus V_{CE} which is having slope -1/Rc.To determine the two points on the line we assume $V_{CE} = V_{CC}$ and $V_{CE} =0$

a) When $V_{CE} =V_{CC}$; $I_C =0$ and we get a point A

b) When $V_{CE}=0$; $I_C=V_{CC}/R_C$ and we get a point B

The figure below shows the output characteristic curves for the transistor in CE mode. The DC load line is drawn on the output characteristic curves. **Load line -** To draw load line, we have to find saturation current and the cutoff voltage.

Saturation point

The point at which the load line intersects the characteristic curve near thecollector current axis is referred to as the **saturation point** . At this point of time, the current through the transistor is maximum and the voltage across collector is minimum for a given value of load. So, saturation current for the fixed bias circuit, **Ic (sat) =Vcc/Rc** .

Cutoff point

The point where the load line intersects the cutoff region of the collector curvesis referred as the cutoff point (i.e. end of load line). At this point, collector current is approximately zero and emitter is grounded for fixed bias circuit. so, **Vce (cut) = Vc = VccOperating point** - The **"Q point"** for a transistor amplifier circuit is the point along itsoperating region in a "quiescent ", where no input signal gets amplified.

The figure below shows the output characteristic curves for the transistor in CE mode with points A and B, and line drawn between them. The line drawn between points A and B is called d.c load line. The d.c word indicates that only d.c conditions are considered, i.e input signal is assumed to be zero. The d.c load line is a plot of I_C versus V_{CE}. For a given value of Rc and a given value of Vcc. So, it represents all

collector current levels and corresponding collector emitter voltages that can exist in the circuit. Knowing any one of Ic, I_B, or V_{CE} , it is easy to determine the other two from the load line. The slope of the d.c load line depends on the value of R_C. It is the negative and equal to reciprocal of the R_C.

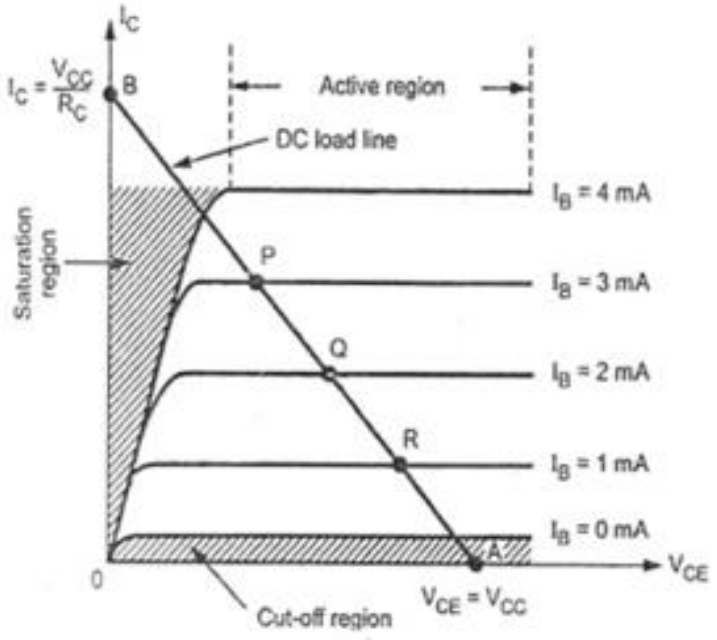


Figure 1.3.2 The output characteristic curves for the transistor in CE mode with points A and B

Diagram Source Brain Kart

Applying KVL to the base circuit, we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$
$$I_B R_B = V_{CC} - V_{BE}$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The intersection of curves of different values I_B of with d.c load line gives different operating points. For different values of I_B, we have different intersection points such as P, Q and R.

Selection of operating point

The operating point can be selected at different positions on the d.c load line, near saturation region, near cut-off region or at the centre, i.e in the active region. The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the d.c. load line to prevent any possible distortion in the amplified output signal.

Output Characteristics

When the output characteristics of a transistor are considered, the curve looks as below for different input values. In the figure 1.3.2 , the output characteristics are drawn between collector current $\mathbf{I_C}$ and collector voltage $\mathbf{V_{CE}}$ for different values of base current $\mathbf{I_B}$. These are considered here for different input values to obtain different output curves.

Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure 1.3.3 below.

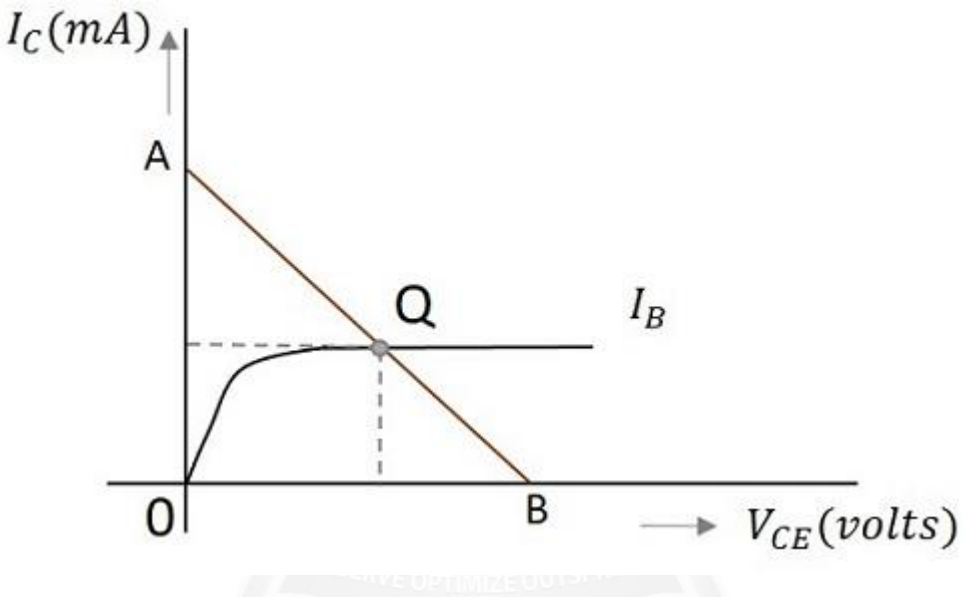


Figure 1.3.3 The Q Point or Operating Point

Diagram Source Brain Kart

The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input. This is discussed in AMPLIFIERS tutorial.

DC Load line

When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as **DC** condition. Here there will be no amplification as the signal is absent. The circuit will be as shown below figure 1.3.4.

The value of collector emitter voltage at any given time will be

$$VCE=VCC-ICRCVCE=VCC-ICRC$$

As V_{CC} and R_C are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure 1.3.5 below shows the DC load line.

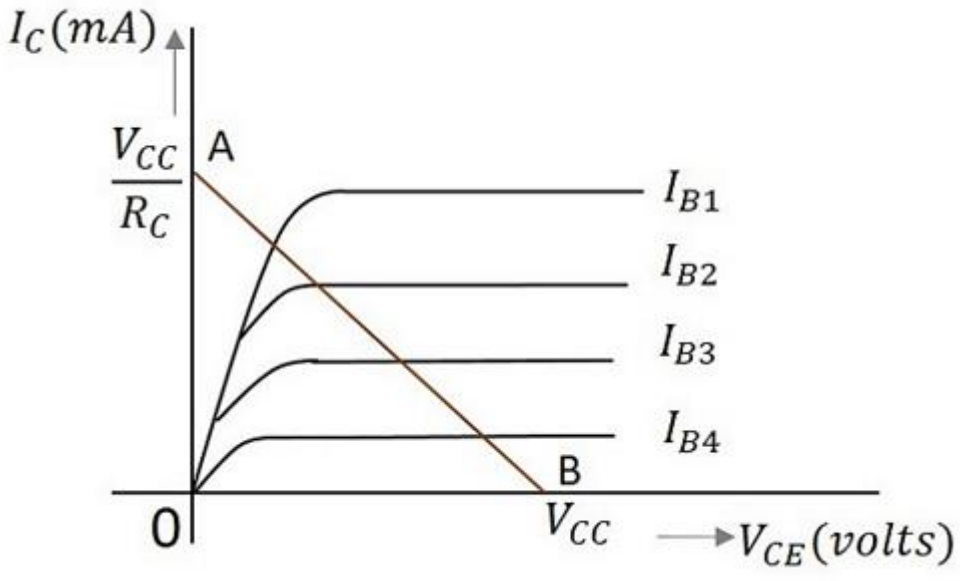


Figure 1.3.5 DC load line

Diagram Source Brain Kart

To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

When collector emitter voltage V_{CE} = 0, the collector current is maximum and is equal to V_{CC}/R_C. This gives the maximum value of V_{CE}. This is shown as

$$VCE=VCC−ICRCVCE=VCC−ICRC$$

$$0=VCC−ICRC0=VCC−ICRC$$

$$IC=VCCRCIC=VCCRC$$

This gives the point A ($OA = V_{CC}/R_C$) on collector current axis, shown in the above figure 1.3.5.

To obtain B

When the collector current IC = 0, then collector emitter voltage is maximum and will be equal to the VCC. This gives the maximum value of IC. This is shown as

$$VCE=VCC−ICRCVCE=VCC−ICRC$$

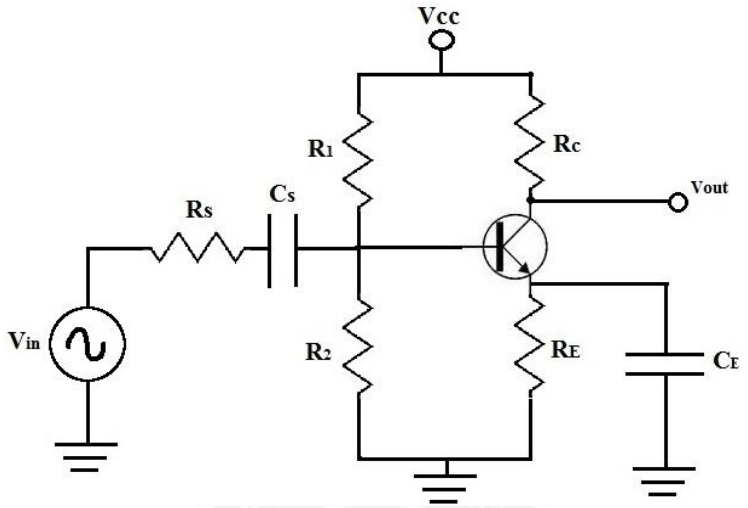
$$=VCC=VCC$$

(As $I_C = 0$)

This gives the point B, which means ($OB = V_{CC}$) on the collector emitter voltage axis shown in the above figure 1.3.5.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn as shown in the figure 1.3.5.

DC Analysis of a Bipolar Junction Transistor Circuit



DC Analysis

When doing DC analysis, all AC voltage sources are taken out of the circuit because they're AC sources. DC analysis is concerned only with DC sources. We also take out all capacitors because in DC, capacitors function as open circuits. For this reason, everything before and after capacitors are removed, which in this circuit includes resistor, Rs , Below figure 1.3.1 is the schematic of the circuit above with respective to DC analysis:

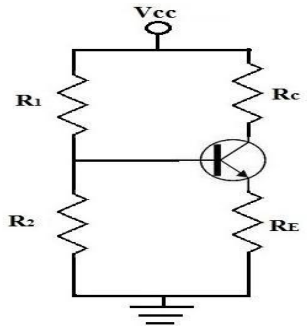


Figure 1.3.1 Circuit for DC analysis

Diagram Source Brain Kart

Now let's do the calculations to find the Vbb, Rb, Ieq, and Vceq. From this then, we can find the quiescient or just simply Q-point of this transistor circuit.

$$V_{bb} = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_B = R_1 \parallel R_2 = \frac{(R_1)(R_2)}{R_1 + R_2}$$

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{(\beta+1)} + R_E}$$

$$V_{CEQ} = V_{cc} - I_{EQ}(R_C + R_E)$$

$$\text{Q-point} = (V_{CEQ}, I_{EQ})$$