UNIT II

EMBEDDEDNETWORKING

2.7 SERIAL BUS COMMUNICATION PROTOCOLS–USB

USB Host Applications Connecting

- flash memory cards,
- pen-like memory devices,
- digital camera,
- printer,
- mouse-device,
- Pocket PC,
- videogames,
- Scanner

Universal Serial Bus (USB)

_Serial transmission and reception between host and serial devices

_The data transfer is off our types: (a) Controlled data transfer, (b) Bulk data transfer, (c)Interrupt driven data transfer,(d) Iso - synchronous transfer

_ A bus between the host system and interconnected number of peripheral devices

USB Protocol Features

_Maximum 127 devices can connect a host.

_ Three standards: USB1.1 (alowspeed1.5 Mbps 3 meter channel along with a high speed 12Mbps 25 meter channel),USB2.0 (high speed 480 Mbps 25 meter channel),and wireless USB(high speed 480Mbps 3 m)

Host connection to the devices or nodes

_ Using USB port driving software and host controller,

_Host computer or system has a host controller which connects to a root hub.

_ A hub is one that connects to other nodes or hubs.

_ A tree-like topology
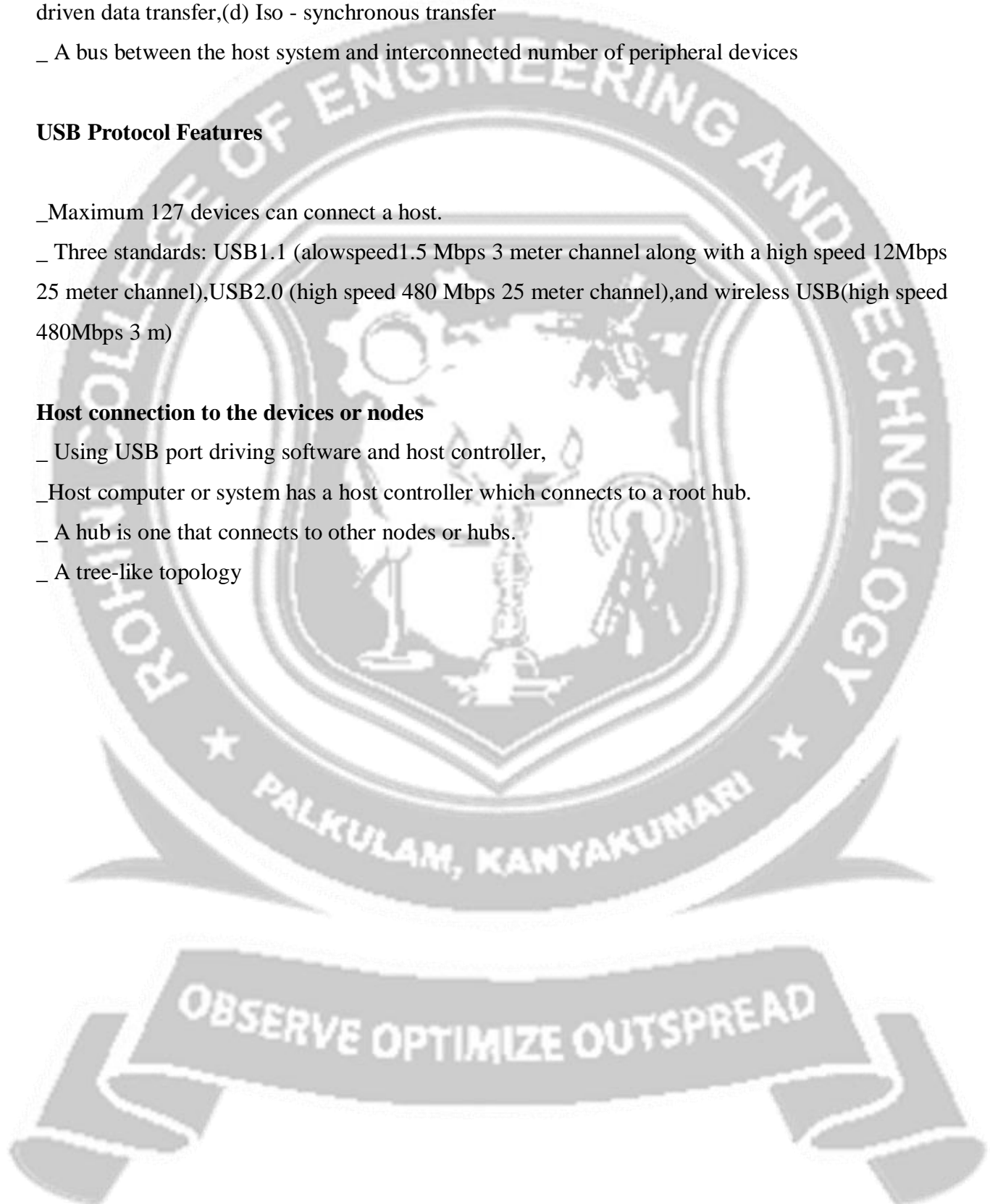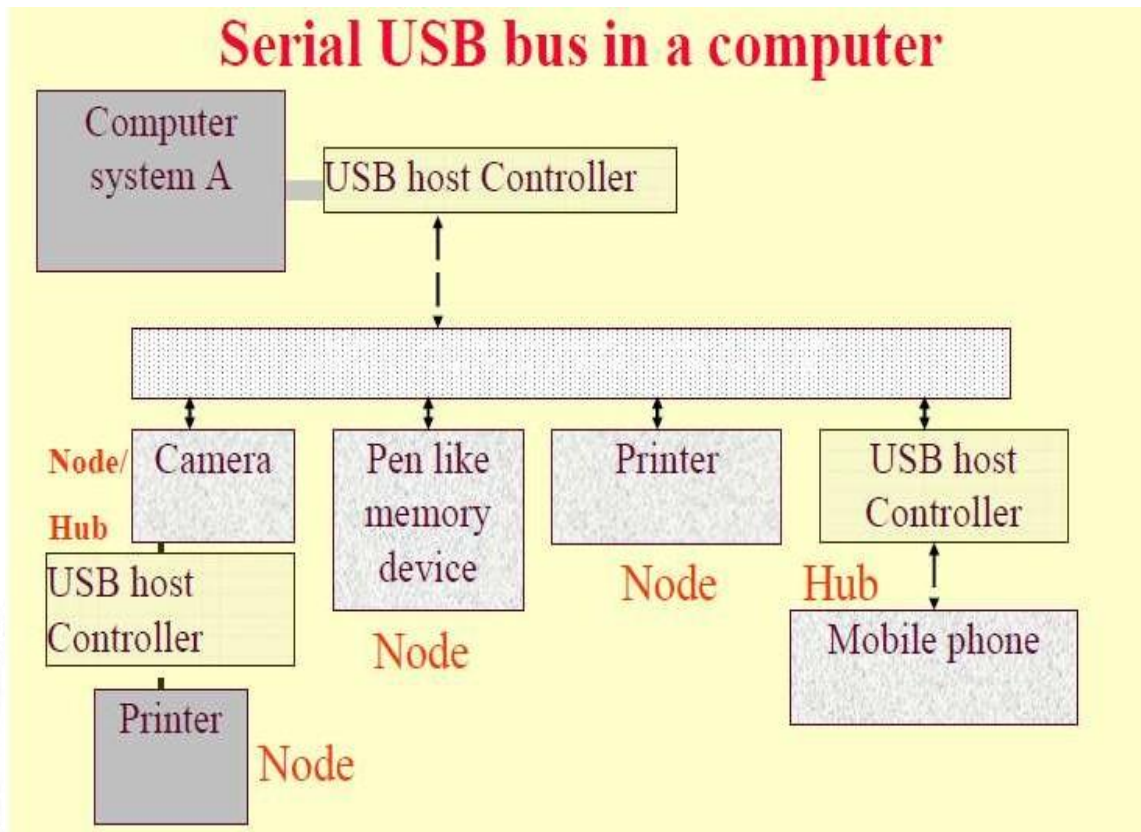
USB Device features

_ Can be hot plugged (attached), configured and used, reset, reconfigured and used

_ Bandwidth sharing with other devices: Host schedules the sharing of bandwidth among

the attached devices at an instance.

_Can be detached (while others are in operation) and reattached.

_ Attaching and detaching USB device or host without rebooting

USB device descriptor

_ Has data structure hierarchy as follows:

_It has device descriptor at the root which has number of configuration descriptors, which has

number of interface descriptor and which has number of end point descriptor.

Powering USB device

_A device can be either bus-powered or self-powered.

_In addition, there is a power management by software at the host for USB ports

USB protocol

_USB bus cable has four wires, onefor+5V, two for twisted pairs and one for ground.

_Termination impedances at each end as per the device-speed.

_Electromagnetic Interference (EMI)- shielded cable for the 15 Mbps USB devices.

_Serial signals NRZI (Non Return to Zero (NRZI)

_ The synchronization clock encoded by inserting synchronous code (SYNC) field before each USB packet

_Receiver synchronizes its bits recovery clock continuously

USB Protocol

• A polled bus

• Host controller regularly polls the presence of a device as scheduled by the software.

• It sends a token packet.

• The token consists of fields for type, direction, USB device address and device end-point number.

• The device does the hand shaking through a hand shake packet, indicating successful run successful transmission.

• ACRC field in a data packet permits error detection

USB supported three types of pipes

1. 'Stream' with no USB- defined protocol. It is used when the connection is already established and the data flow starts

2. 'Default Control 'for providing access.

3. 'Message 'for the control functions for of the device.

• Host configures each pipe with the data band width to be used transfer service type and buffer sizes.

PARALLEL BUS DEVICE PROTOCOLS –PCI Bus

_Parallel bus enables a host computer or system to communicate simultaneously

32-bit or 64-bit with other devices or systems, for example, to a network interface card (NIC) or graphic card

Computer system PCI

• When the I/O devices in the distributed embedded sub systems are networked all can communicate   through a common parallel bus.

• PCI connects at high speed to other sub systems having a range of I/O devices at very short distances (<25 cm) using a parallel bus without having to implement a specific interface for each I/O device.

PCI bus Applications

Connects

_ display monitor,

_printer,

_character devices,

_network sub systems,

_video card,

_modem card,

_hard disk controller,

PCI bus connects

_thin client,

_digital video capture card,

_streaming displays,

_10/100 Base T card,

_Card with16 MB Flash ROM with a router gate way for a LAN and

_Card using DEC21040PCIE the net LAN controller.

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PCI Bus Feature

_ 32- bit data bus extendible to 64 bits.

_PCI protocol specifies the ways of interaction between the different components of a computer.

_A specification version 2.1 ─ synchronous / asynchronous through put is up to 132/528MB/s[33M ×4/ 66M×8 Byte/s], operates on 3.3V to 5Vsignals.

_ PCI driver can access the hardware automatically as well as by the programmer assigned addresses.

_ Automatically detects the interfacing systems and assigns new addresses

_Thus simplified addition and deletion (attachment and detachment) of the system peripherals.

FIFO in PCI device/card

_ Each device may use a FIFO controller with a FIFO buffer for maximum through put Identification Numbers

_ A device identifies its address space by three identification numbers, (i) I/O port (ii) Memory locations and (iii) Configuration registers of total 256Bwith a four 4-byte unique ID. Each PCI device has address space allocation of256 bytes to access it by the host Computer

PCI device identification

_A sixteen16-bit register in a PCI device identifies this number to let that device auto-detect it.

_ Another sixteen16-bit register identifies a device ID number. These two numbers let allow the device to carry out its auto-detection by its host computer.

Peripheral Component Interconnect(PCI)Bus

_Independent from the IBM architecture.

_Number of embedded devices in a computer system use PCI

_ Three standards for the devices interfacingwith the PC

_ PCI32bit/33 MHz and 64bit/66MHz

_ PCI Extended (PCI/X)64 bit/100MHz,

_ Compact PCI (cPCI) Bus

Two super speed versions

_PCI Super V2.3 264/528 MBps   3.3V (on64- bit bus), and 132/264 (on 32-bitbus)and

_PCI-X SuperV1.01afor 800MBps 64- bit bus 3.3Volt.

PCI bridge

_ PCI bus interface switches a process or communication with the memory bus to PCI bus.

_In most systems the processor has a single data bus that connects to a switch module

_ Some processors integrate the switch module onto the same integrated circuit as the processor to reduce the number of chips required to build a system and thus the system cost.

_ Communicates with the memory through a *memory bus* (a set of address, control and data buses),a dedicated set of wires that transfer data between these two systems.

_A separate *I/O bus* connects the PCI switch to the I/O devices.

Advantage of Separate memory and I/O buses

_ I/O system generally designed for maximum flexibility, to allow as many different I/O devices as possible to interface to the computer

_ Memory bus is designed to provide the maximum-possible bandwidth between the processor and the memory system.

PCI-X (PCI extended)

• 133MBps to as much as 1GBps

• Backward compatible with existing

PCI cards

• Used in high bandwidth devices(Fiber Channel, and processors that are part of a cluster and Giga bit Ether net)

• Maximum 264 MBps through put,uses8,16,32,or64bit transfers

• 6U cards contain additional pins for user defined I/Os

• Live insertion support (Hot-Swap),

• Supports two independent buses on the back plane(on different connectors)

• Supports Ethernet, Infinite band, and Star Fabric support (Switched fabric based

systems) **Compact PCI (cPCI)**

Each PCI device on Bus

_Perform a specific function,

_ May contain a processor and software to perform a specific function.

_ Each device has the specific memory address- range, specific interrupt-vectors(pre-

assigned or auto configured) and the device I/O port addresses.

_ A bus of appropriate specifications and protocol interfaces these to the host computer

system or computer

Configuration address space

_ Unique feature of PCI bus unique feature is its configuration address space.

PCI controller Features

• Accesses one device at a time

• All the devices within host device or system can share the I/O port and memory addresses
but

Cannot share the configuration registers

• Device cannot modify other configuration registers but can access other device resources
or share

the work or assist the other device

• If there are reasons for doing it so, a PCI driver can change the default boot up

assignments on configuration transactions.

PCI Device Initialization

A device can initialize at booting time

• Avoids any address collision

• Device on boot up disables its interrupt and closes its door to its address space except to
the

Configuration registers space

PCIBIOS (Basic Input-Output System)
Performs the configuration transactions and then, memory and address spaces automatically map to
the address space in the device hosting