DIGITAL TECHNIQUES IN HIGH VOLTAGE MEASUREMENT

Resistance Potential Dividers

The resistance potential dividers are the first to appear because of their simplicity of construction, less space requirements, less weight and easy portability. These can be placed near the test object which might not always be confined to one location. The length of the divider depends upon two or three factors. The maximum voltage to be measured is the first and if height is a limitation, the length can be based on a surface flash over gradient in the order of 3–4 kV/cm irrespective of whether the resistance R1 is of liquid or wire wound construction. The length also depends upon the resistance value but this is implicitly bound up with the stray capacitance of the resistance column, the product of the two (RC) giving a time constant the value of which must not exceed the duration of the wave front it is required to record. It is to be noted with caution that the resistance of the potential divider should be matched to the equivalent resistance of a given generator to obtain a given wave shape.

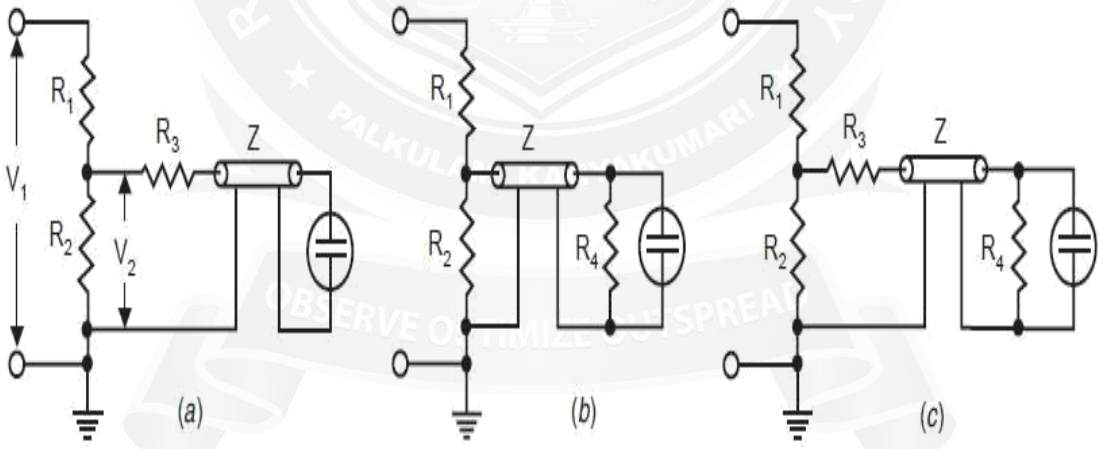

Figure 4.5.1 various forms of resistance potential dividers recording circuits

[Source: "High Voltage Engineering" by C.L. Wadhwa , Page – 438]

Here R_3, the resistance at the divider end of the delay cable is chosen such that $R_2 + R_3$ =

Z which puts an upper limit on R_2 i.e., R2 < Z. In fact, sometimes the condition for matching is given as

$$Z = R3 + \frac{R1R2}{R1+R2}$$

But, since usually $R_1 > > R_2$, the above relation reduces to $Z = R_3 + R_2$.

$$V2 = \frac{Z1}{Z1+R1} V1$$

where Z_1 is the equivalent impedance of R_2 in parallel with $(Z + R_3)$, the surge impedance of the cable being represented by an impedance Z to ground.

$$Z1 = \frac{(Z+R3)R2}{R2+Z+R3} = \frac{(Z+R3)R2}{2Z}$$

Therefore,

$$V2 = \frac{(Z+R3)R2}{2Z} \frac{V1}{Z1+R1}$$

$$V3 = \frac{V2}{Z+R3} Z = \frac{Z}{Z+R3} \frac{(Z+R3)R2}{2Z} . \frac{V1}{Z1+R1} = V1 \frac{R2}{2(Z1+R1)}$$

However, the voltage entering the delay cable is

As this voltage wave reaches the CRO end of the delay cable, it suffers reflections as the impedance offered by the CRO is infinite and as a result the voltage wave transmitted into the CRO is doubled. The CRO, therefore, records a voltage The reflected wave, however, as it reaches the low voltage arm of the potential divider does not suffer any reflection as $Z = R_2 + R_3$ and is totally absorbed by $(R_2 + R_3)$. Since R_2 is smaller than Z and Z_1 is a parallel combination of R_2 and $(R_3 + Z)$, Z_1 is going to be smaller than R_2 and since $R_1 > > R_2$, R_1 will be much greater than Z_1 and, therefore to a first approximation $Z_1 + R_1 \approx$

R_1.

Therefore,

$$V_3' = \frac{R2}{R1}V1 \approx \frac{R2}{R1+R2}V1 \text{ as } R2 << R1$$

cable Matching is done by a pure ohmic resistance $R_4 = Z$ at the end of the delay cable and, therefore, the voltage reflection coefficient is zero i.e. the voltage at the end of the cable is transmitted completely into R4 and hence appears across the CRO plates without being reflected. As the input impedance of the delay cable is $R_4 = Z$, this resistance is a parallel to R2 and forms an integral part of the divider's low voltage arm. The voltage of such a divider is, therefore, calculated as follows: Equivalent impedance

$$R1 + \frac{R2Z}{RZ+Z} = \frac{R1(R2+Z)+R2Z}{(R2+Z)}$$

$$I = \frac{V1(R2+Z)}{R1(R2+Z)+R2Z}$$

Therefore, Current

$$V2 = \frac{IR2Z}{R2+Z} = \frac{V1(R2+Z)}{R1(R2+Z)+R2Z}\frac{R2Z}{R2+Z}$$

$$= \frac{R2Z}{R1(R2+Z)+R2Z}V1$$

$$\frac{V2}{V1} = \frac{R2Z}{R1(R2+Z)+R2Z}$$

Due to the matching at the CRO end of the delay cable, the voltage does not suffer any reflection at that end and the voltage recorded by the CRO is given as

$$V2 = \frac{R2}{2R1+R2}V1$$

For a given applied voltage V_1 this arrangement will produce a smaller deflection on

the CRO Plates as compared to the one in Figure. The arrangement of Figure) provides for matching at both ends of the delay cable and is to be recommended where it is felt necessary to reduce to the minimum irregularities produced in the delay cable circuit. Since matching is provided at the CRO end of the delay cable, therefore, there is no reflection of the voltage at that end and the voltage recorded will be half of that recorded in the arrangement of ,

$$V2 = \frac{R2}{2(R1+R2)} V1$$

It is desirable to enclose the low voltage resistance (s) of the potential dividers in a metal screening box. Steel sheet is a suitable material for this box which could be provided with a detachable closefitting lid for easy access. If there are two low voltage resistors at the divider position as in Figure they should be contained in the screening box, as close together as possible, with a removable metallic partition between them. The partition serves two purposes (i) it acts as an electrostatic shield between the two resistors (ii) it facilitates the changing of the resistors. The lengths of the leads should be short so

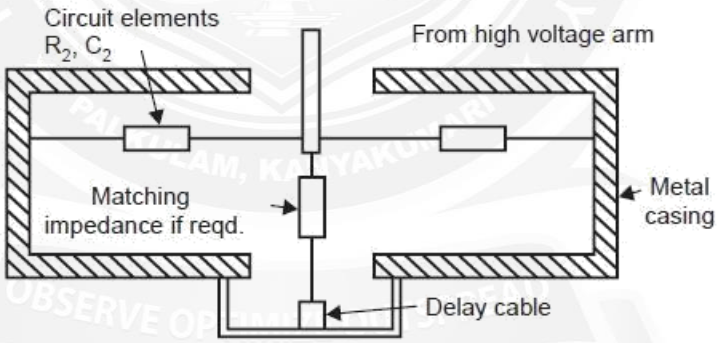

Figure 4.5.2 shows a sketched cross-section of possible layout for the low voltage arm of voltage divider.

[Source: "High Voltage Engineering" by C.L. Wadhwa , Page – 445]

Capacitance Potential Dividers

Capacitance potential dividers are more complex than the resistance type. For measurement of impulse voltages not exceeding 1 MV capacitance dividers can be both portable and transportable. In general, for measurement of 1 MV and over, the capacitance divider is a laboratory fixture. The capacitance dividers are usually made of capacitor units mounted one above the other and bolted together. It is this failure which makes the small dividers portable. A screening box similar to that described earlier can be used for housing both the low voltage capacitor unit C_2 and the matching resistor if required.

The low voltage capacitor C_2 should be non-inductive. A form of capacitor which has given excellent results is of mica and tin foil plate, construction, each foil having connecting tags coming out at opposite corners. This ensures that the current cannot pass from the high voltage circuit to the delay cable without actually going through the foil electrodes. It is also important that the coupling between the high and low voltage arms of the divider be purely capacitive. Hence, the low voltage arm should contain one capacitor only; two or more capacitors in parallel must be avoided because of appreciable inductance that would thus be introduced.

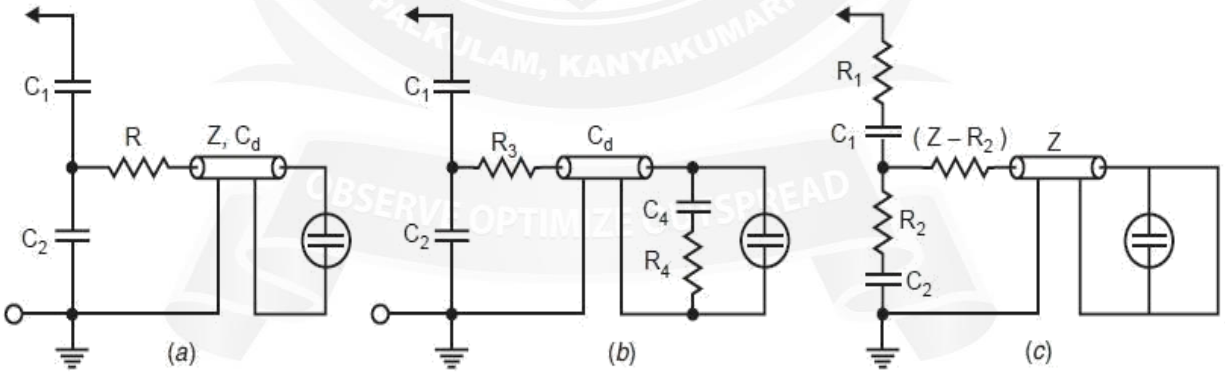

Figure 4.5.3 Capacitor divider

[Source: "High Voltage Engineering" by C.L. Wadhwa , Page – 451]

A low Resistor in parallel to C_2 would load the low voltage arm of the divider too heavily and decrease the output voltage with time. Since R and Z form a potential divider and R = Z, the voltage input to the cable will be half of the voltage across the capacitor C_2. This halved voltages travels towards the open end of the cable (CRO end) and gets doubled after reflection. That is, the voltage recorded by the CRO is equal to the voltage across the capacitor C_2. The reflected wave charges the cable to its final voltage magnitude and is absorbed by R (i.e. reflection takes place at R and since R = Z, the wave is completely absorbed as coefficient of voltage reflection is zero) as the capacitor C2 acts as a short circuit for high frequency waves. The transformation ratio, therefore, changes from the value:

$$\frac{C_1 + C_2}{C_1}$$

for very high frequencies to the value

$$\frac{C_1 + C_2 + C_d}{C_1}$$

However, the capacitance of the delay cable Cd is usually small as compared with C2. For capacitive divider an additional damping resistance is usually connected in the lead on the High voltage side. The performance of the divider can be improved if damping resistor which corresponds to the a periodic limiting case is inserted in series with the individual element of capacitor divider. This kind of damped capacitive divider acts for high frequencies as a resistive divider and for low frequencies as a capacitive divider. It can, therefore, be used over a wide range of frequencies i.e. for impulse voltages of very different duration and also for alternating voltages.