4.4 Differential Mode Operation

In the differential mode, the two input signals are different from each other. Considerthe two input signals which are same in magnitude but 180" out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig.

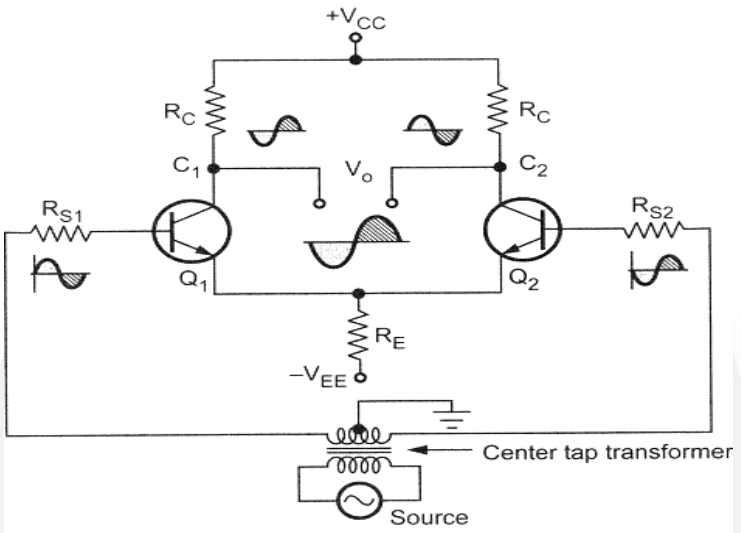


Fig Differential mode operation

Figure: 4.4.1 Differential mode operation

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 145]

Assume that the sine wave on the base of Q 1is positive going while on the base of Q 2 is negative going. With a positive going signal on the base of Q 1, m amplified negative going signal develops on the collector of Q1. Due to positive going signal, current through R E also increases and hence a positive going wave is developed across R E. Due to negative going signal on the base of Q2, an amplified positive going signal develops on the collector of Q 2. And a negative going signal develops across R E, because of emitter follower action of Q 2. So signal voltages across R E, due to the effect of Q1 and Q2 are equal in magnitude and 180o out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance. Hence R E in this case does not introduce negative feedback. While Vo is the output taken across collector of Q1 and collector of Q 2. The two outputs on collector L and 2 are equal in magnitude

but opposite in polarity. And Vo is the difference between these two signals, e.g. +10 - (-10) = + 20.

Hence the difference output Vo is twice as large as the signal voltage from either collector to ground

Common Mode operation

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.

In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across R_E, which add together. Hence R_E carries a signal current and providesa negative feedback. This feedback reduces the common mode gain of differential amplifier.

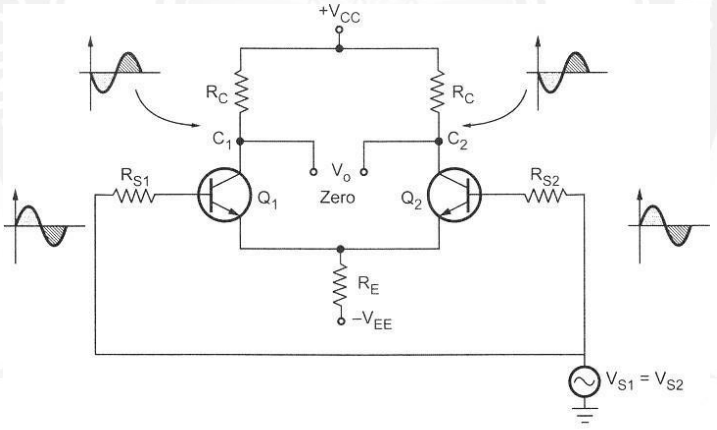


Fig. Common mode operation

Figure: 4.4.2 Common mode operation

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 146]

While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q 1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase,

Eg. (20) - (20) = 0. Thus the difference output Vo is almost zero, negligibly small. Ideally it should be zero.

Configurations of Differential Amplifier

The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations:

i) Dual input balanced output differential amplifier.

ii) Dual input, unbalanced output differential amplifier.

iii) Single input, balanced output differential amplifier.

iv) Single input, unbalanced output differential amplifier.

The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collectors with respect to ground it is called unbalanced output or single ended output. If the signal is given to both the input terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Fig. (a). The dual input, unbalanced output differential amplifier is shown in the Fig.(b). The single input, balanced output differential amplifier is shown in the Fig (c) and the single input, unbalanced output differential amplifier is shown in the Fig. (d).

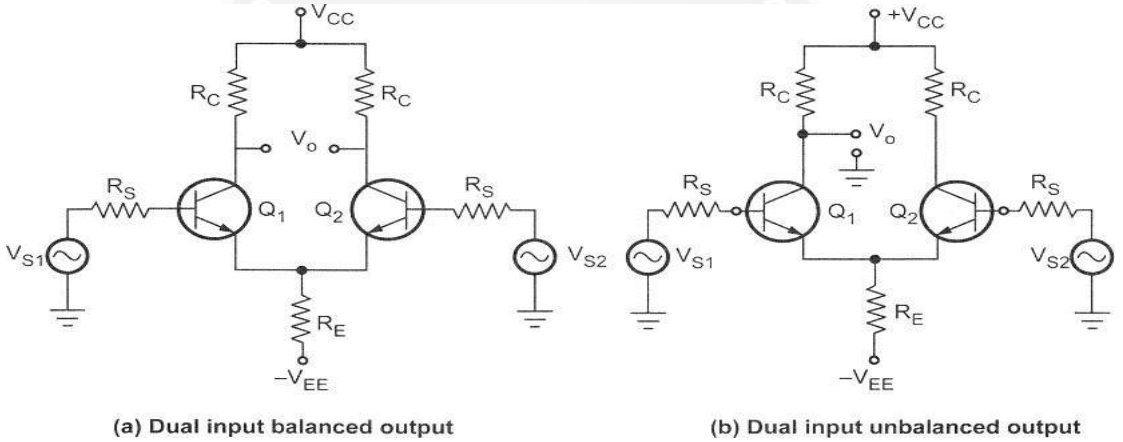
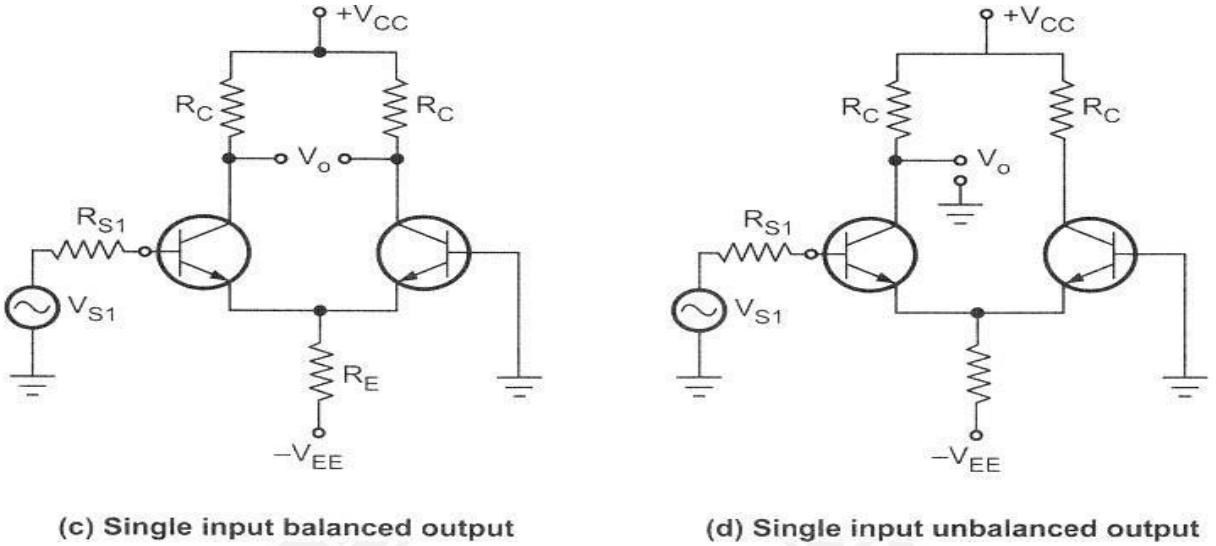


Figure: 4.4.3 Dual input balanced and Dual input unbalanced output

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 146]



(c) Single input balanced output (d) Single input unbalanced output

Figure: 4.4.3 Single input balanced and single input unbalanced output

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 147]