Digital-to-Analog Converter – DAC0800

1. Digital-to-Analog Converters

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Fig :3-bit DAC

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1. R-2-R ladder network and
2. weighted resistor network.

Figure 2.8 Block diagram of a 3-bit DAC

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2. Types of DAC

2.1 R-2R Ladder Network DAC

1. R-2-R ladder network DAC:

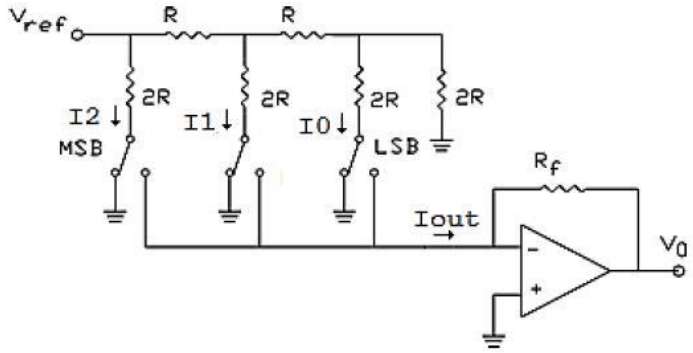


Fig: R-2-R ladder network DAC

Figure 2.9 R-2R ladder network DAC

- Uses only two resistor values, **R** and **2R**.
- Each switch connects its resistor either to the reference voltage or to ground; the switches can be transistors.
- The resistors are connected so that, for any binary input, the total current I_T is proportional to the binary input.
- The op-amp converts the current I_T to a voltage signal V0.

2.2 Weighted Resistor DAC

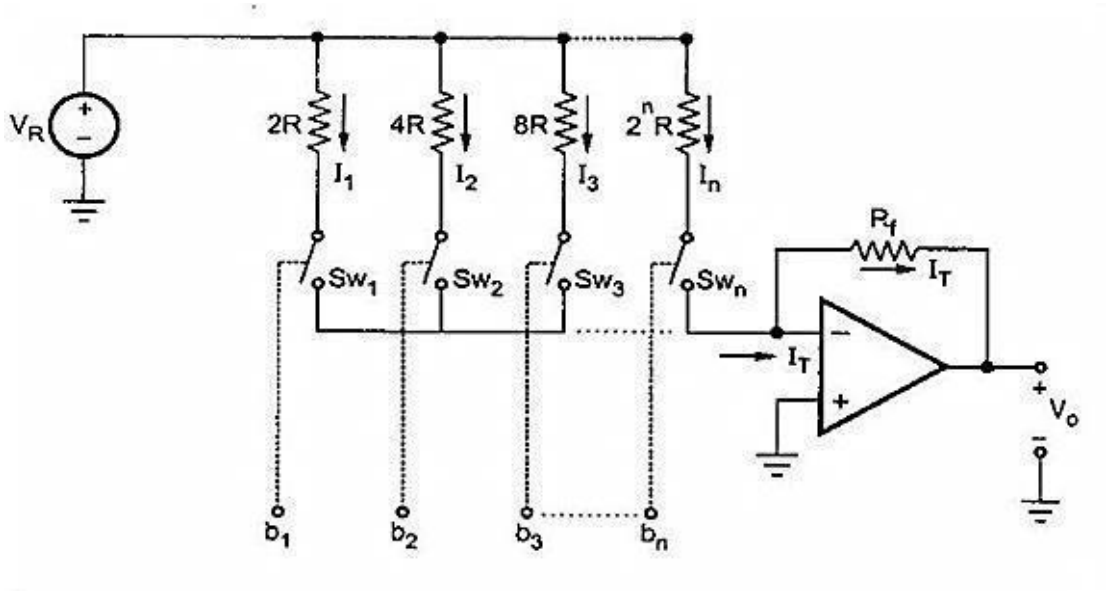


Figure 2.10 Weighted resistor DAC

- Uses an op-amp to sum n binary-weighted currents derived from a reference voltage VR through current-scaling resistors 2R, 4R, 8R … 2^nR.
- The switch positions are controlled by the digital input: when the bit is 1 the resistor is connected to VR, otherwise it is left open. For an ON switch I = VR/R and for an OFF switch I = 0.
- The op-amp acts as a summing amplifier; the total current through Rf is I_f = I1 + I2 + I3 + … + In.
- Output voltage across Rf: **V0 = – I·Rf**.

Feature	R-2R ladder	Weighted resistor
Resistor values	Only R and 2R	2R, 4R, 8R … 2^nR (binary weighted)
Output stage	Op-amp converts total current I_T to voltage V0	Op-amp summing amplifier; V0 = – I·Rf

3. Interfacing DAC0800

3.1 Features

- Monolithic **8-bit** DAC manufactured by National Semiconductor.
- Settling time around 100 ms (as given in the source notes).
- Power supply range 4.5 V to +18 V; usually V+ is 5 V or +12 V; the V− pin can be kept at a minimum of −12 V.
- Resolution of the DAC is 39.06 mV.

3.2 Pin Diagram

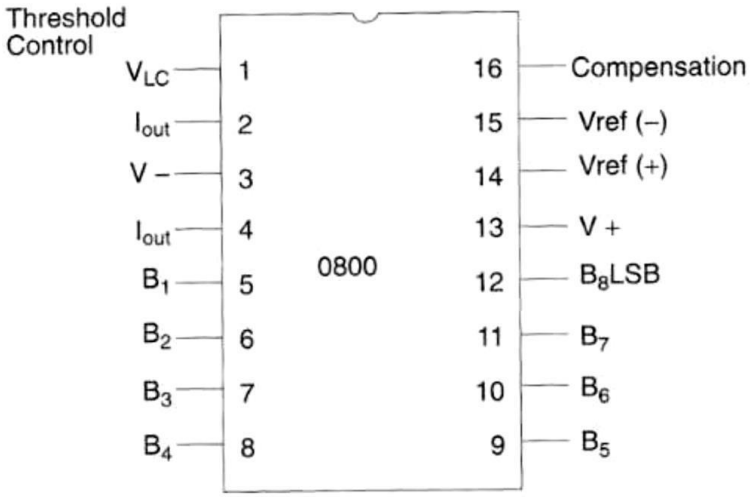


Figure 2.11 DAC0800 pin diagram

Pin	Name	Pin	Name
1	VLC (threshold control)	16	Compensation
2	Iout	15	Vref (−)
3	V−	14	Vref (+)
4	Iout (complement)	13	V+
5	B1 (MSB)	12	B8 (LSB)
6	B2	11	B7
7	B3	10	B6
8	B4	9	B5