16-bit Microprocessor (8086) Features and Architecture:

- 8086 Microprocessor is a 16-bit μp.
- 8086 has a 20 bit address bus can access up to 2^{20} memory locations (1 MB).
- It can support up to 64K I/O ports.
- It provides 14, 16 -bit registers.
- Word size is 16 bits and double word size is 4 bytes.
- It has multiplexed address and data bus AD0- AD15 and A16 – A19.
- It requires single phase clock with 33% duty cycle to provide internal timing.
- 8086 is designed to operate in two modes, Minimum and Maximum.
- It can pre fetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution.
- It requires +5V power supply.
- A 40 pin dual in line package.
- Address ranges from 00000H to FFFFFH
- Memory is byte addressable - Every byte has a separate address.

Internal Architecture of 8086:

8086 has two blocks BIU and EU. The BIU handles all transactions of data and addresses on the buses for EU. The BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands. The instruction bytes are transferred to the instruction queue. EU executes instructions from the instruction system byte queue.

Both units operate asynchronously to give the 8086 an overlapping instruction fetch and execution mechanism which is called as Pipelining. This results in efficient use of the system bus and system performance. BIU contains Instruction queue, Segment registers, Instruction pointer, and Address adder. EU contains Control circuitry, Instruction decoder, ALU, Pointer and Index register, Flag register.

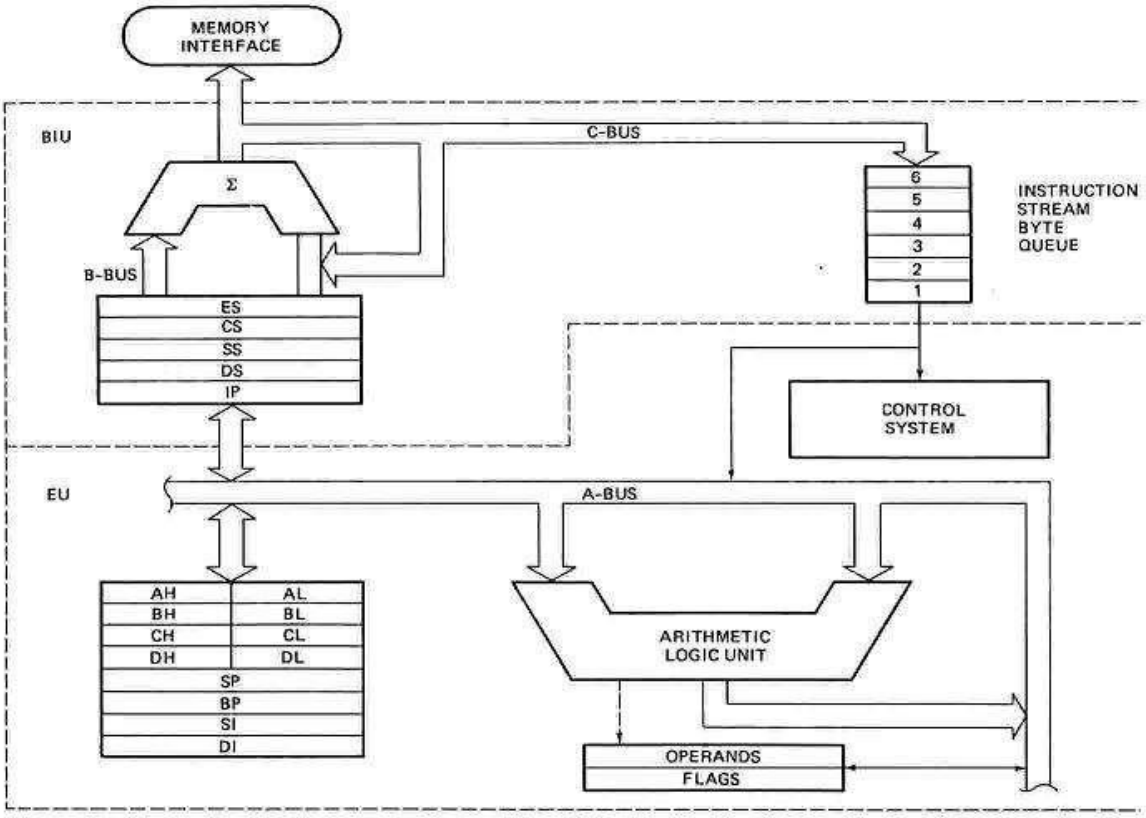


FIGURE 8086 internal block diagram. (*Intel Corp.*)

1. Bus Interface Unit (BIU)

The BIU handles all data, address, and control signal transfers between the microprocessor and external devices.

Functions:

- Fetches instructions from memory.
- Calculates physical addresses using segment and offset.
- Queues instructions for the Execution Unit.

  Components:
- **Segment Registers**:
  - **CS** (Code Segment) – Stores code segment address.
  - **DS** (Data Segment) – Stores data segment address.
  - **SS** (Stack Segment) – Stack operations.
  - **ES** (Extra Segment) – Additional data storage.
- **Instruction Pointer (IP)** – Holds offset of the next instruction.
- **Instruction Queue** – 6-byte FIFO queue for pre fetching instructions.

2. Execution Unit (EU)

The EU executes instructions fetched by the BIU.

Functions:

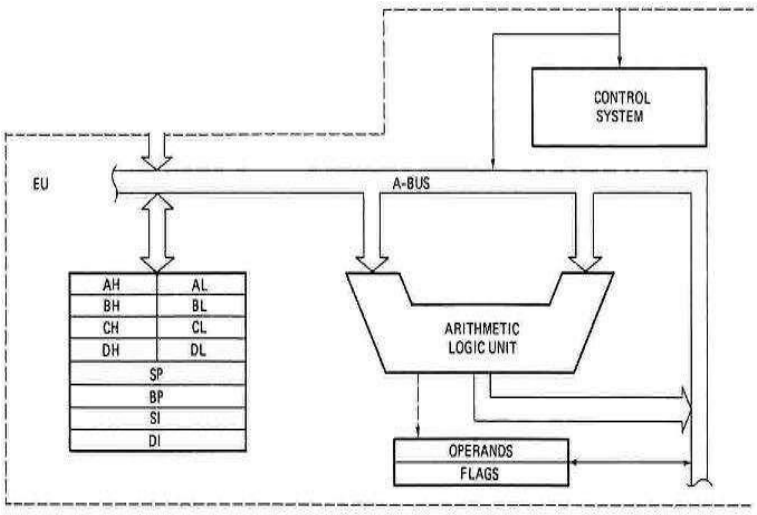
- Decodes and executes instructions.
- Controls ALU operations.
- Manages flag register.

Components:

- **ALU (Arithmetic Logic Unit)** – Performs arithmetic and logic operations.
- **General Purpose Registers**: AX, BX, CX, DX (each can be split into high and low bytes).
- **Pointer and Index Registers**: SP, BP, SI, DI.
- **Flag Register** – Holds status flags (e.g., Zero, Carry, Sign, Overflow).
- **Control Unit** – Directs operation flow.

EXECUTION UNIT

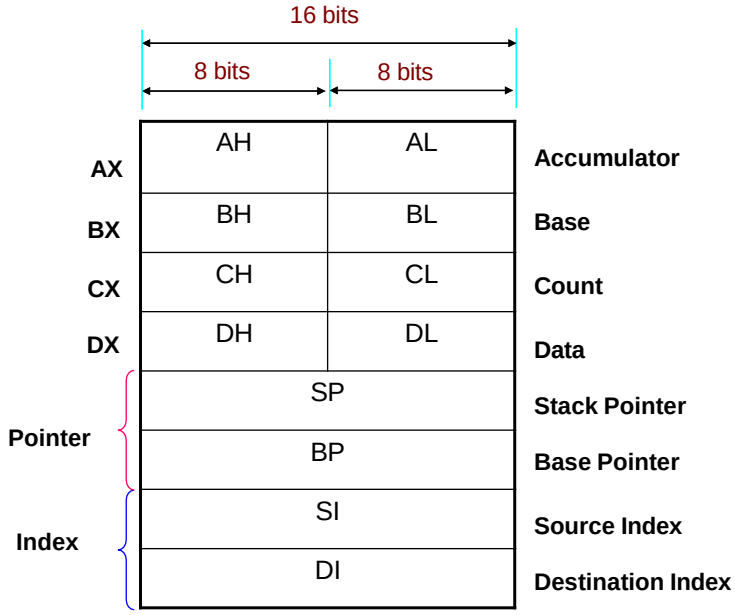
- Decodes instructions fetched by the BIU
- Generate control signals,
- Executes instructions.



The main parts are:

- Control Circuitry
- Instruction decoder
- ALU

EXECUTION UNIT – General Purpose Registers



EXECUTION UNIT – General Purpose Registers

Register	Purpose
AX	Word multiply, word divide, word I /O
AL	Byte multiply, byte divide, byte I/O, decimal arithmetic
AH	Byte multiply, byte divide
BX	Store address information
CX	String operation, loops
CL	Variable shift and rotate
DX	Word multiply, word divide, indirect I/O (Used to hold I/O address during I/O instructions. If the result is more than 16-bits, the lower order 16-bits are stored in accumulator and higher order 16-bits are stored in DX register)

Pointer and Index Registers

- Used to keep offset addresses.
- Used in various forms of memory addressing.
- In the case of SP and BP the default reference to form a physical address is the Stack

Segment (SS- will be discussed under the BIU)

- The index registers (SI & DI) and the BX generally defaults to the Data segment register (DS).

SP: Stack pointer

– Used with SS to access the stack segment

BP: Base Pointer

– Primarily used to access data on the stack

– Can be used to access data in other segments

SI: Source Index register

- is required for some string operations
- When string operations are performed, the SI register points to memory locations in the data segment which is addressed by the DS register. Thus, SI is associated with the DS in string operations.

DI: Destination Index register

- is also required for some string operations.
- When string operations are performed, the DI register points to memory locations in the data segment which is addressed by the ES register. Thus, DI is associated with the ES in string operations.
- The SI and the DI registers may also be used to access data.

Flag Register

The 8086 **flag register** is a **16-bit register** used to indicate the current status of the processor and to control certain operations.

It has **two types of flags:**

1. **Status Flags** – Indicate the result of arithmetic or logic operations.
2. **Control Flags** – Control the processor's operation.

1. Status Flags

Flag	Meaning	Set When
CF (Carry Flag)	Indicates carry/borrow in arithmetic	Carry out from MSB or borrow into MSB
PF (Parity Flag)	Indicates parity of result	Set if number of 1's in LSB is even
AF (Auxiliary Carry Flag)	For BCD operations	Carry from bit 3 to bit 4
ZF (Zero Flag)	Shows if result is zero	Set if result = 0
SF (Sign Flag)	Shows sign of result	Set if MSB = 1 (negative)
OF (Overflow Flag)	Indicates signed overflow	Set if signed result exceeds range

2. Control Flags

Flag	Meaning	Use
TF (Trap Flag)	Single-step mode	Debugging
IF (Interrupt Flag)	Enables interrupts	Set to allow maskable interrupts
DF (Direction Flag)	String operation direction	0 = increment, 1 = decrement