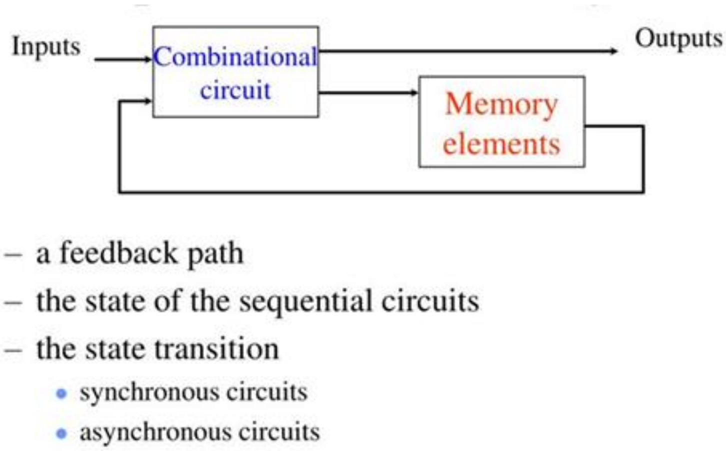
Sequential Circuits

Sequential circuits are a type of digital circuit that store and use previous state information to determine their next state. They consist of input variables, logic gates (combinational circuits), and output variables. The memory elements in sequential circuits can be implemented using flip-flops, which store binary values and maintain their state even when the inputs change.



Flip Flops

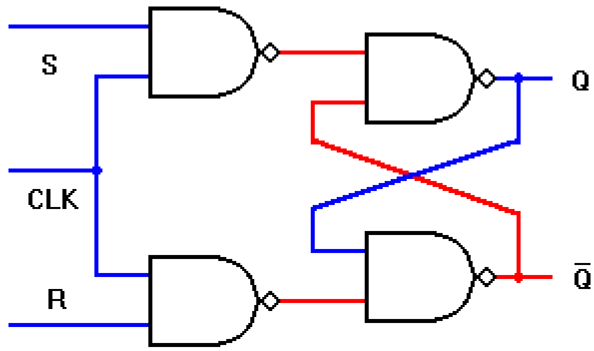
A digital computer needs devices that can store information. A flip-flop is a binary storage device. It can store binary bits either 0 or 1. It has two stable states HIGH and LOW i.e. 1 and 0. It has the property to remain in one state indefinitely until it is directed by an input signal to switch over to the other state.

The basic function of the flip-flop is to store data. They can be used to keep a record of the value of a variable (input, output, or intermediate). They are also used to exercise control over the functionality of a digital circuit i.e. change the operation of a circuit depending on the state of one or more flip flops. These devices are mainly used in situations that require one or more of these three. Operations, storage, and sequencing.

RS Flip Flop

The RS latch flip flop required direct input but no clock. It is very use full to add a clock to control precisely the time at which the flip-flop changes the state of its output.

In the clocked R-S flip flop the appropriate levels applied to their inputs are blocked till the receipt of a pulse from another source called a clock. The flip-flop changes state only when the clock pulse is applied depending upon the inputs. The basic circuit is shown in Figure 2. This circuit is formed by adding two AND gates at inputs to the R-S flip flop. In addition to control inputs Set (S) and Reset (R), there is a clock input (C) also.



The excitation table for R-S flip flop is very simply derived as given below

Excitation table for R-S Flip Flop

S	R	Q
0	0	No Change
0	1	Reset (0)
1	0	Set (1)
1	1	Indeterminate

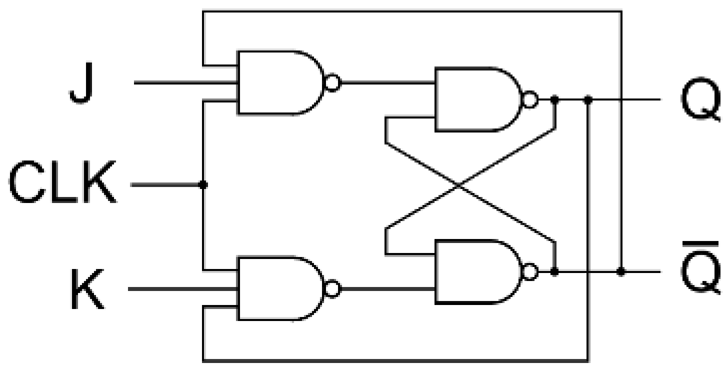
The truth table for the Clocked R-S flip flop

Initial Conditions	Inputs (Pulsed)		Final Output	Comment
Q	S	R	Q (t + 1)	No Change
0	0	0	0	No Change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	???	indeterminate
1	0	0	1	No Change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	???	indeterminate

JK Flip Flop

One of the most useful and versatile flip flops is the JK flip flop the unique features of a JK flip flop are:

1. If the J and K input are both at 1 and the clock pulse is applied, then the output will change state, regardless of its previous condition.
2. If both J and K inputs are at 0 and the clock pulse is applied there will be no change in the output. There is no indeterminate condition, in the operation of the JK flip flop i.e. it has no ambiguous state. The circuit diagram for this is shown in Figure 4.



JK Flip Flop

When J = 0 and K = 0

These J and K inputs disable the NAND gates, therefore clock signals have no effect on the flip flop. In other words, Q returns its last value.

When J = 0 and K = 1,

The upper NAND gate is disabled the lower NAND gate is enabled if Q is 1 therefore, the flip flop will be reset (Q = 0 , Q =1)if not already in that state.

When J = 1 and K = 0

The lower NAND gate is disabled and the upper NAND gate is enabled if Q is at 1, As a result, we will be able to set the flip flop (Q = 1, Q= 0) if not already set

When J = 1 and K = 1

If Q = 0 the lower NAND gate is disabled the upper NAND gate is enabled. This will set the flip flop and hence Q will be 1. On the other hand, if Q = 1, the lower NAND gate is enabled and the flip flop will be reset hence Q will be 0. In other words, when J and K are both high, the clock pulses cause the JK flip-flop to toggle. The truth table for the JK flip-flop is shown in Table.

The excitation table for JK or SR flip flop is very simply derived as given in table

Excitation table for JK Flip Flop

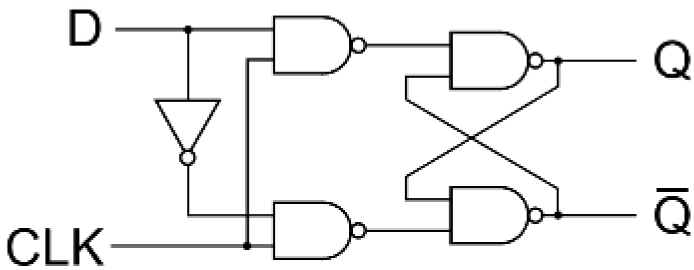
S	R	Q
0	0	No Change
0	1	0
1	0	1
1	1	Toggle

The truth table for the JK flip flop

Initial Conditions	Inputs (Pulsed)		Final Output
Q	S	R	Q (t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

D Flip Flop

A D type (Data or delay flip flop) has a single data input in addition to the clock input as shown in Figure.



Basically, such type of flip flop is a modification of clocked RS flip flop gates from a basic Latch flip flop, and NOR gates modify it into a clock RS flip flop. The D input goes directly to the S input and its complement through the NOT gate, is applied to the R input.

This kind of flip-flop prevents the value of D from reaching the output until a clock pulse occurs. The action of the circuit is straightforward as follows.

When the clock is low, both AND gates are disabled, therefore D can change values without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced equal to D when the clock again goes low, and Q retains or stores the last value of D. The truth table for such a flip-flop is as given below in Table.

Truth table for D Flip Flop

S	R	Q(t + 1)
0	0	0
0	1	1
1	0	0
1	1	1

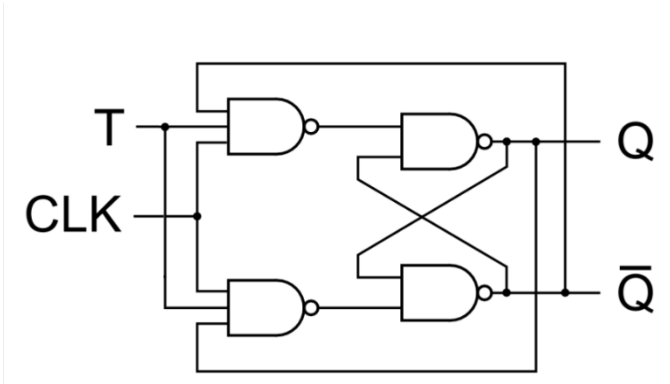
The excitation table for D flip flop is very simply derived given as under.

Excitation table for D Flip Flop

S	Q
0	0
1	1

T Flip Flop

A T Flip-Flop is a type of digital logic device that allows for rapid, reliable data transmission. It relies on NAND Gates, which are digital logic devices containing two inputs and one output. The operation of the T Flip-Flop is based on the Boolean operation: when both inputs are high, the output is low.



To draw the circuit diagram of a T Flip-Flop using the NAND Gate, it's important to first understand how NAND Gates operate. Each NAND Gate has two inputs (A and B) and one output (Y). When both of the inputs are high, then the output is low. Additionally, if either input is low, the output will be high. With this understanding, we can now draw our circuit diagram.

The circuit diagram consists of two NAND Gates. The output of the first NAND Gate is connected to the input of the second NAND Gate. The output of the second NAND Gate is then connected to the input of the first NAND Gate. This creates a looping circuit, which constantly monitors the inputs and outputs. If both inputs are high, then the output is low, which forms the basis for the T Flip-Flop.

In summary, the T Flip-Flop is an essential part of digital logic that allows for rapid, reliable data transmission. It relies on two NAND Gates, whose inputs and outputs must be correctly connected in order to properly form the looping circuit.

Characteristics Table for the Toggle Function

CLK	T	Q	Q+1
_↑‾	0	0	0
_↑‾	0	1	1
_↑‾	1	0	1
_↑‾	1	1	0