## FLIP FLOPS

A latch is an essential component in the construction of an edge-triggered register. It is level-sensitive circuit that passes the D input to the Q output when the clock signal is high. This latch is said to be in transparent mode. When the clock is low, the input data sampled on the falling edge of the clock is held stable at the output for the entire phase, and the latch is in hold mode. A latch operating under the above conditions is a positive latch.

**Flip flops Principle:**

Static memories use positive feedback to create a bistable circuit — a circuit having two stable states that represent 0 and 1. The basic idea is shown in below figure which shows two inverters connected in cae along with a voltage-transfer characteristic typical of such a circuit. Also plotted are the VTCs of the first inverter, that is,$V_{o1}$ versus $V_{i1}$, and the second inverter ($V_{o2}$ versus $V_{o1}$).
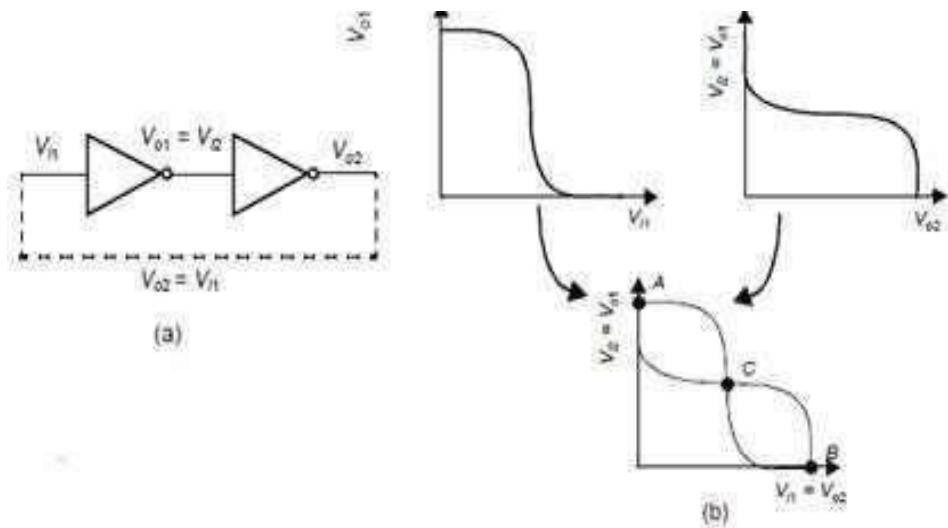


**Fig 3.2.1: Example of H-tree clock distribution**

[Source : Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective …]

The latter plot is rotated to accentuate that $Vi2 = Vo1$. Assume now that the output of the second inverter $Vo2$ is connected to the input of the first $Vi1$, as shown by the dotted lines in Figure 7.4a. The resulting circuit has only three possible operation points (A, B, and C), as demonstrated on the combined VTC.

**Multiplexer Based Flip flops**

There are many approaches for constructing latches. One very common technique involves the use of transmission gate multiplexers. Multiplexer based latches can provide similar functionality to the SR latch, but has the important added advantage that the sizing of devices only affects performance and is not critical to the functionality. Figure 7.11 shows an implementation of static positive and negative latches based on multiplexers.

For a negative latch, when the clock signal is low, the input 0 of the multiplexer is selected, and the D input is passed to the output. When the clock signal is high, the input 1 of the multiplexer, which connects to the output of the latch, is selected. The feedback holds the output stable while the clock signal is high. Similarly in the positive latch, the D input is selected when clock is high, and the output is held (using feedback) when clock is low.
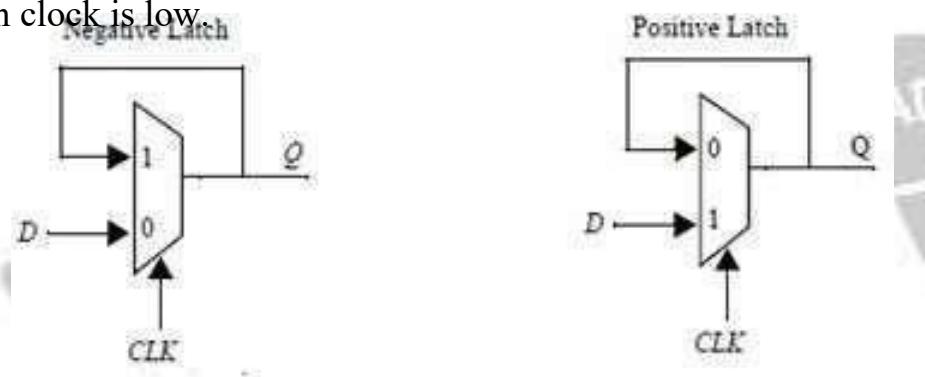


**Fig 3.2.2: Negative and Positive Flip flops based on multiplexer**

[Source : Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated

Circuits:A Design perspective …]

A transistor level implementation of a positive latch based on multiplexers is shown in figure. When CLK is high, the bottom transmission gate ison and the latch is transparent - that is, the D input is copied to the Q output. During this phase, the feedback loop is open since the top transmission gate is off.
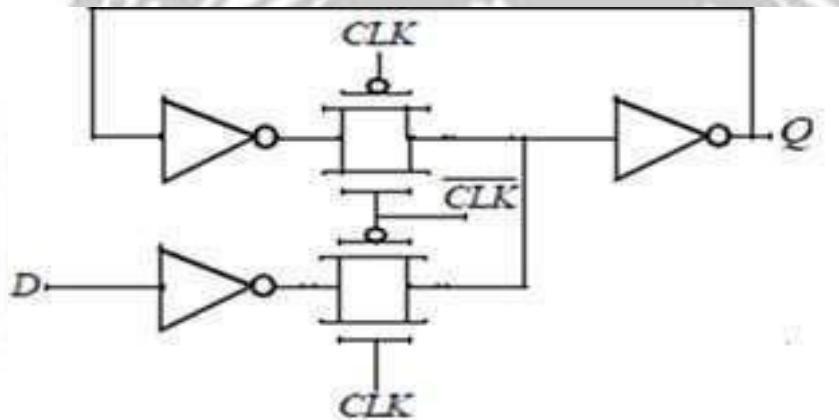


**Fig 3.2.3: Transistor level implementation of a positive** Flip flops **built using transmission gates**
[Source : Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated

Circuits:A Design perspective …]

Unlike the SR FF, the feedback does not have to be overridden to write the memory and hence sizing of transistors is not critical for realizing correct functionality. The number of transistors that the clock touches is important since it has an activity factor of 1. This particular latch implementation is not particularly efficient from this metric as it presents a load of 4 transistors to the CLK signal.

It is possible to reduce the clock load to two transistors by using implement

multiplexers using NMOS only pass transistor as shown in Figure 3.2.4 The advantage of this approach is the reduced clock load of only two NMOS devices. When CLK is high, the latch samples the D input, while a low clock-signal enables the feedback-loop, and puts the latch in the hold mode.

### Low-Voltage Static Flip flops

The scaling of supply voltages is critical for low power operation. Unfortunately, certain latch structures don't function at reduced supply voltages. For example, without the scaling of device thresholds, NMOS only pass transistors don't scale well with supply voltage due to its inherent threshold drop. At very low power supply voltages, the input to the inverter cannot be raised above the switching threshold, resulting in incorrect evaluation. Even with the use of transmission gates, performance degrades significantly at reduced supply voltages.Scaling to low supply voltages hence requires the use of reduced threshold
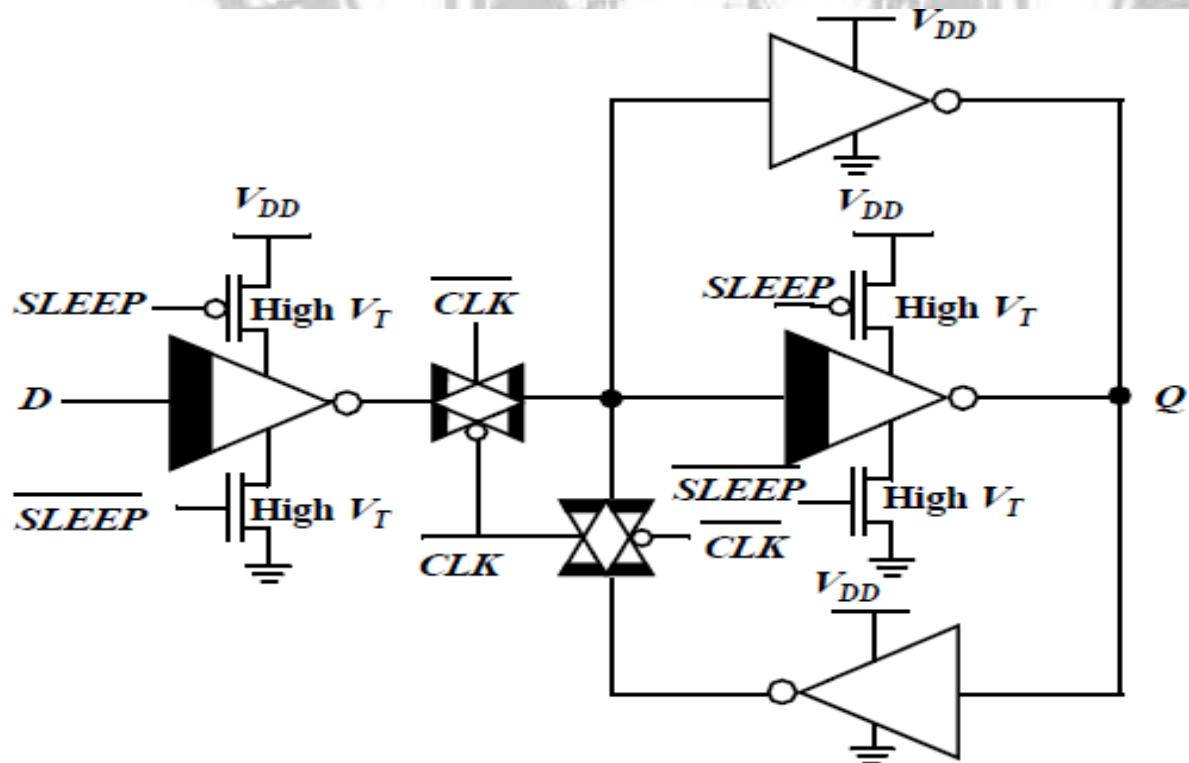


**Fig 3.2.4: one solution for the leakage problem in low-voltage operation using MTCMOS**

devices. However, this has the negative effect of exponentially increasing the sub- threshold leakage Power. age energy is typically insignificant compared to the switching power. However, with the use of conditional clocks, it is possible that registers are idle for extended periods and the leakage energy expended by registers can be quite significant.

Many solutions are being explored to address the problem of high leakage during idle periods. One approach for this involves the use of Multiple Threshold devices as shown in above figure only the negative latch is shown here. The shaded inverters and

transmission gates are implemented in low-threshold devices. The low threshold inverters are gated using high threshold devices to eliminate leakage.

During normal mode of operation, the sleep devices are tuned on. When clock is low, the D input is sampled and propagates to the output. When clock is high, the latch is in the hold mode. The feedback transmission gate conducts and the cross-coupled feedback is enabled. Note there is an extra inverter, needed for storage of state when the latch is in the sleep state. During idle mode, the high threshold devices in series with the low threshold inverter are turned off (the SLEEP signal is high), eliminating leakage. It is assumed that clock is in the high state when the latch is in the sleep state. The feedback low-threshold transmission gate is turned on and the cross-coupled high-threshold device maintains the state of the latch.