3.8.SYNCHRONOUS COUNTERS:

Flip-Flops can be connected together to perform counting operations. Such a group of Flip- Flops is a **counter**. The number of Flip-Flops used and the way in which they are connected determine the number of states (called the modulus) and also the specific sequence of states that the counter goes through during each complete cycle.

Counters are classified into two broad categories according to the way they are clocked:

- Asynchronous counters,
  Synchronous counters.

In asynchronous (ripple)counters, the first Flip- Flop is clocked by the external clock pulse and the each successive Flip- Flop is clocked by the output of the preceding Flip-Flop.

In synchronous counters, the clock input is connected to all of the Flip-Flops so that they are clocked simultaneously. With in each of these two categories, counters are classified primarily by the type of sequence, the number of states, or the number of Flip-Flops in the counter.

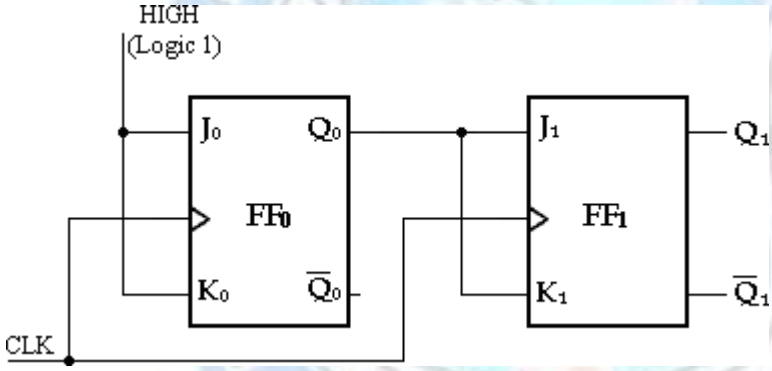
The term synchronous refers to events that have a fixed time relationship with each other. In synchronous counter, the clock pulses are applied to all Flip Flop simultaneously. Hence there is minimum propagation delay.

S.No	Asynchronous(ripple)counter	Synchronouscounter
1	All the Flip-Flops are not clocked simultaneously.	All the Flip-Flops are clocked simultaneously.
2	The delay time so fall Flip-Flops are added. Therefore there is considerable propagation delay.	There is minimum propagation delay.
3	Speed of operation is low	Speed of operation is high.
4	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of state increases.

5	Minimum numbers of logic devices are needed.	The number of logic devices is more than ripple counters.
6	Cheaper than synchronous counters.	Costlier than ripple counters.

2- Bit Synchronous Binary Counter

In this counter the clock signal is connected in parallel to clock input so both the Flip-Flops (FF0 and FF1). The output of FF0 is connected to J1 and K1 inputs of the second Flip- Flop(FF1).



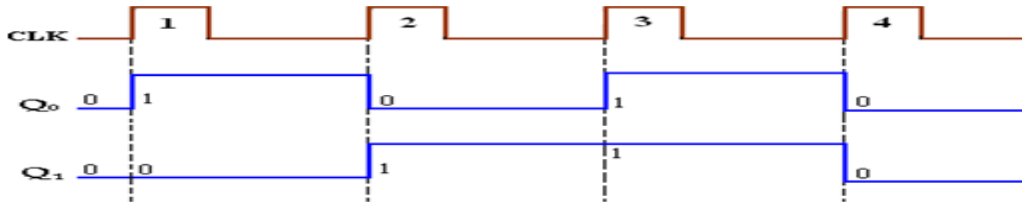
2-BitSynchronousBinaryCounter

Assume that the counter is initially in the binary 0 state: i.e., both Flip-Flopsare RESET. When the positive edge of the first clock pulse is applied, FF0 will toggle because J0= k0= 1, whereas FF1 output will remain 0 because J1= k1=0. After the first clock pulseQ0=1andQ1=0.

When the leading edge of CLK2 occurs, FF0 will toggle and Q0 will go LOW.Since FF1 has a HIGH (Q0 = 1) on its J1 and K1 inputs at the triggering edgeof this clock pulse, the Flip-Flop toggles and Q1goes HIGH.Thus, after CLK2, Q0=0andQ1=1.

When the leading edge of CLK3 occurs, FF0 again toggles to the SET state(Q0= 1), and FF1 remains SET (Q1 = 1) because its J1 and K1 inputs are both LOW (Q0= 0). After this triggering edge, Q0=1 and Q1=1.

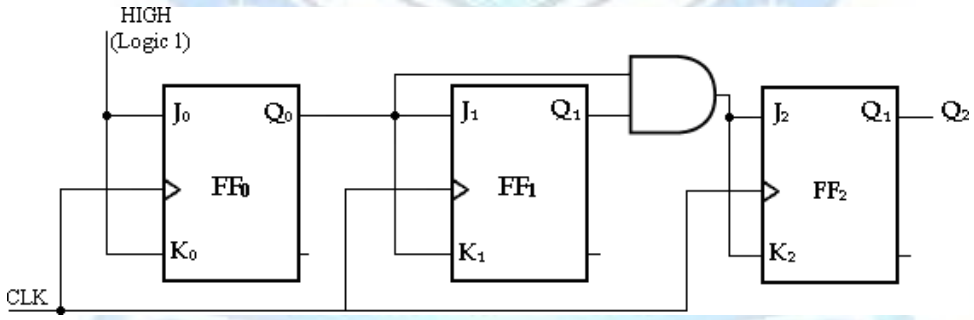
Finally, at the leading edge of CLK4, Q0 and Q1 go LOW because they both have a toggle condition on their J1 and K1 inputs. The counter has now recycled to its original state, Q0=Q1=0.



Timing diagram

3- Bit Synchronous Binary Counter:

A 3 bit synchronous binary counter is constructed with three JK Flip-Flops and an AND gate. The output of FF0 (Q0) changes on each clock pulse as the counterprogresses from its original state to its final state and then back to its original state.To produce this operation, FF0 must be held in the toggle mode by constant HIGH,onitsJ0andK0inputs.



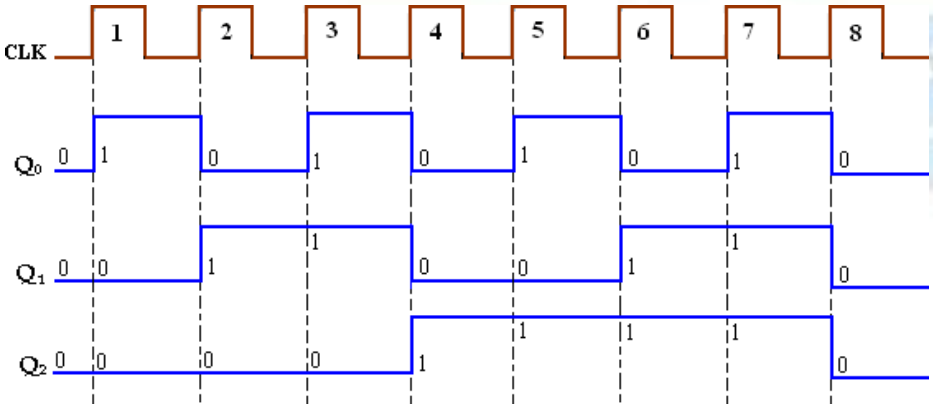
BitSynchronous Binary Counter

The output of FF1 (Q1) goes to the opposite state following each time Q0= 1.This change occurs at CLK2, CLK4, CLK6, and CLK8. The CLK8 pulse causes thecounter to recycle. To produce this operation, Q0 is connected to the J1 and K1 inputs of FF1. When Q0= 1 and a clock pulse occurs, FF1 is in the toggle mode and

therefore changes state. When Q0= 0, FF1 is in the no-change mode and remains in its presentstate.

The output of FF2 (Q2) changes state both times; it is preceded by the unique condition in which both Q0 and Q1 are HIGH. This condition is detected by theAND gate and applied to the J2 and K2 inputs of FF2. Whenever both outputs Q0= Q1=1,the output of the AND gate makes the J2= K2= 1 and FF2 toggles on thefollowing clock pulse. Otherwise, the J2 and K2 inputs of FF2 are held LOW by the AND gate output, FF2 does not change state.

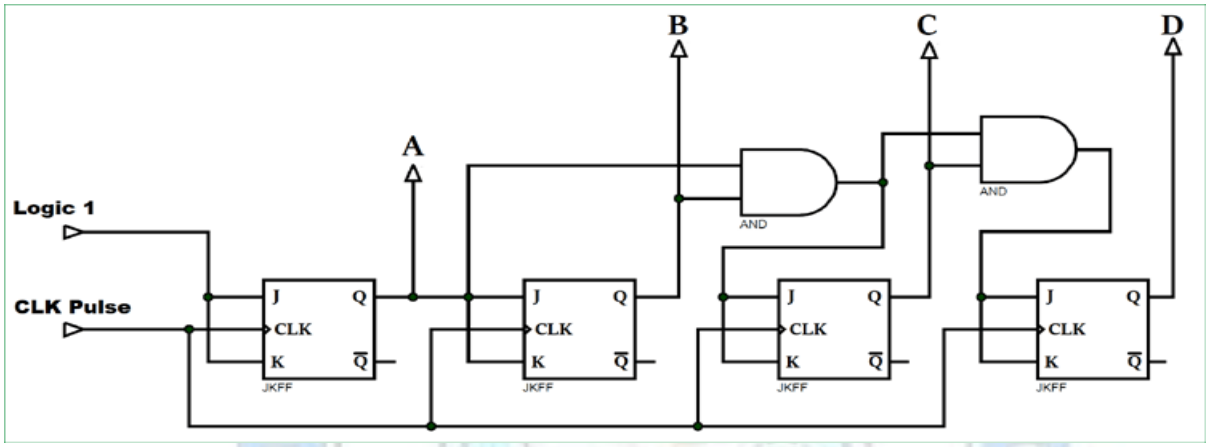
CLOCKPulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8(recycles)	0	0	0



Timing diagram

4- Bit Synchronous Binary Counter

This particular counter is implemented with negative edge-triggered Flip Flops. The reasoning behind the J and K input control for the first three Flip- Flops is the same as previously discussed for the 3-bit counter. For the fourth stage, the Flip-Flop has to change the state when Q0=Q1=Q2=1.This condition is decoded by AND gate G2



Bit Synchronous Binary Counter

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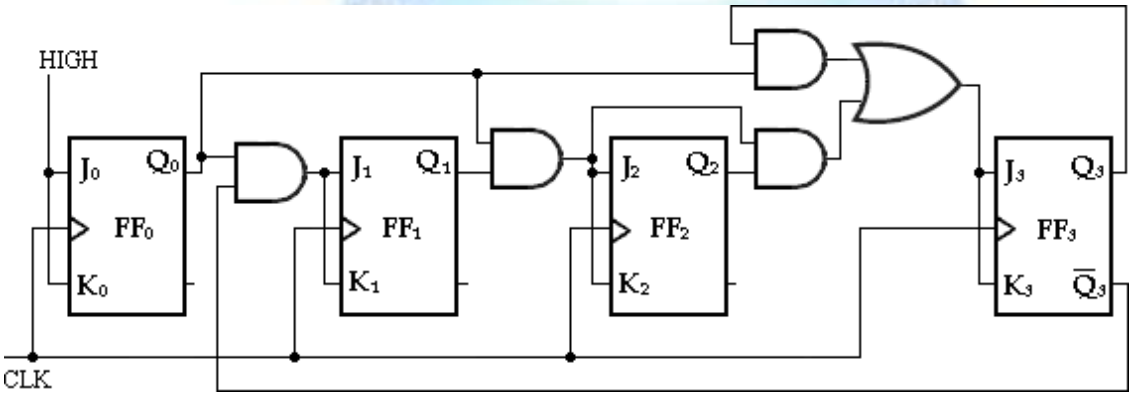
4- Bit Synchronous Decade Counter:(BCDCounter):

BCD decade counter has a sequence from 0000 to 1001(9). After 1001 state it must recycle back to 0000 state. This counter requires four Flip-Flops and AND/OR logic as shown below



Synchronous UP/DOWN Counter

An up/down counter is a bidirectional counter, capable of progressing in either direction through a certain sequence. A3- bit binary counter goes through the sequence in the opposite direction(7,6,5,4,3,2,1,0)is an illustration of up /down sequential operation.

The complete up/down sequence for a 3-bit binary counter is shown in table below.The arrows indicate the state-to-State movement of the counter for both its UPand its DOWN modes of operation. An examination of Q_0 for both the up and down sequences shows that FF_0 toggles on each clock pulse. Thus, the J_0 and K_0 inputs of FF_0 are,

$J_0=K_0=1$

CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

To form asynchronous UP/DOWN counter,the control input (UP/DOWN) is used to allow it the normal output or the inverted output of one Flip-Flop to the J and K inputs of the next Flip-Flop. When UP/DOWN= 1, the MOD 8 counter will count from000to111 and UP/DOWN= 0,itwillcount from 111to000.

When UP/DOWN= 1, it will enable AND gates 1 and 3and disable AND gates 2 and 4. This allows the Q0 and Q1 outputs through the AND gates to the J and K

inputs of the following Flip-Flops, so the counter counts up as pulses are applied.