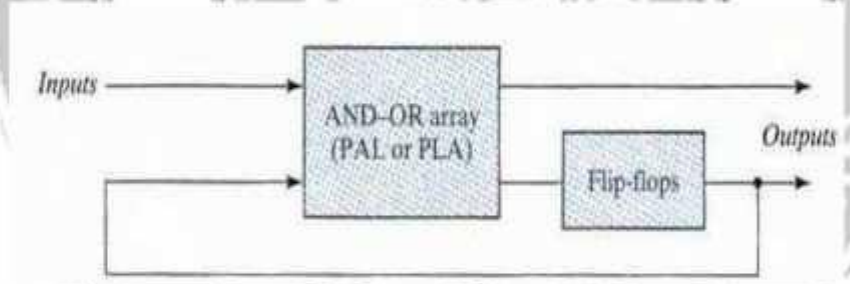
5.2.SEQUENTIAL PROGRAMMABLE DEVICES

Digital systems are designed with flip-flops and gates. Since the combinational PLD consists of only gates, it is necessary to include external flip-flops when they are used in the design. Sequential programmable devices include both gates and flip-flops. In this way, the dev ice can be programmed to perform a variety of sequential-circuit functions.

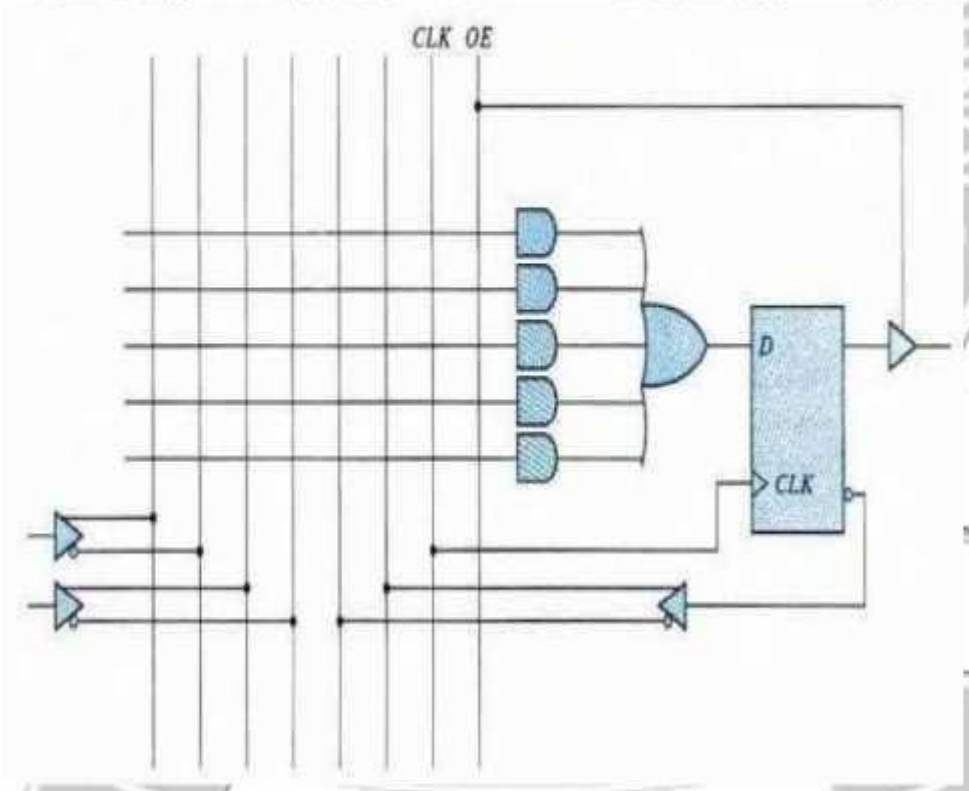
1. Sequential (or simple) programmable logic device (SPLD)
2. Complex programmable logic device (CPLD)
3. Field-programmable gate array (FPGA)



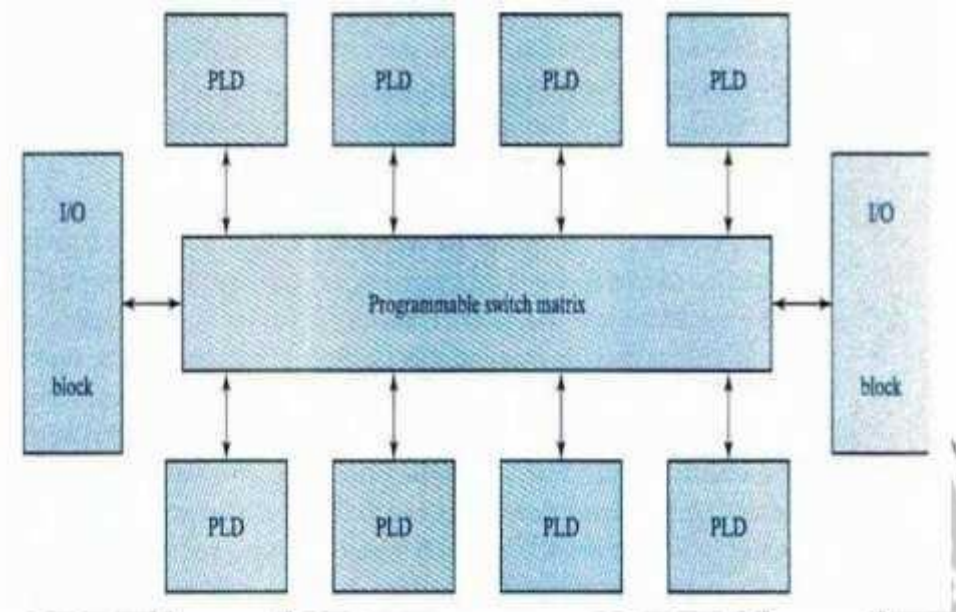
The sequential PLD is sometimes referred 10as a simple PLD to differentiate it from the complex PLD. The SPLD includes flip-flops, in addition to the AND-OR array, within the integrated circuit chip. The result is a sequential circuit as shown in Fig. 7.18. A PAL or PLA is modified by including a number of flip-flops connected to for a register, The circuit outputs can be taken from the OR gates or from the outputs of the flip-flops. Additional programmable connections are available to include the flip-flop outputs in the product terms formed with the AND array. The flip-flops may be of the D or the JK type. The first programmable device developed to support sequential circuit implementation is the fieldprogrammable logic sequencer (FPLS). A typical FPLS is organized around a PLA with several outputs driving flip- flops. The flip-flops are flexible in that they can be programmed to operate as either the JK o r the D type. The FPLS did not succeed commercially,

because it has too many programmable connections. The configuration mostly used in an SPLD is the combinational PAL together with D flip-flops. A PAL that includes flip -flops is referred to as a registered PAL, to signify that the device contains flip-flops in addition to the AND-DR array.

Each section of an SPLD is called a macrocell, which is a circuit that contains a sum- of-products combinational logic function and an optional flip-flop. The output is driven by an edge-triggered D flip-flop connected to a common clock input and changes state on a clock edge. The output of the flipflop is connected to a three- state buffer (or inverter) controlled by an output-enable signal marked in the diagram as OE. The output of the flip -flop is fed back into o ne of the inputs of the programmable AND gates to provide the present-state condition for the sequential circuit. A typical SPLD has from 8 to 10 macrocells within one IC package. All the flip -flop s are connected to the common CLK input, and all three-Male buffers are controlled by the OE input.



The design of a digital system using PLDs often requires the connection of several devices to produce the complete specification. For this type of application, it is more economical to use a complex programmable logic device (CPLD), which is a collection of individual PLDs on a single integrated circuit. A programmable interconnection structure allows the PLDs to be connected to each other in the same way that can be done with individual PLDs.



The device consists of multiple PLDs interconnected through a programmable switch matrix. The input-output blocks provide the connections to the IC pins. Each I/O pin is driven by a three-state buffer and can be programmed to act as input or output, the switch matrix receives inputs from the I/O block and directs them to the individual microcells. Similarly, selected outputs from macrocells are sent to the outputs as needed. Each PLD typically contains from 8 to 16 macrocells, usually fully connected. If a microcell has unused product terms, they can be used by other nearby macrocells. In some cases the macrocell flip-flop is programmed to act as a D, JK or T flip-flop.

A field-programmable gate array (FPGA) is a VLSI circuit that can be programmed at the user's location. A typical FPGA consists of an array of hundreds or thousands of logic blocks, surrounded by programmable input and output blocks and connected together via programmable interconnections. There is a wide variety of internal configurations within this group of devices. The performance of each type of device depends on the circuit contained in its logic blocks and the efficiency of its programmed interconnections.

APPLICATION SPECIFIC INTEGRATED CIRCUITS

Application Specific Integrated Circuit (ASIC) is an integrated circuit(IC) customized for a particular use, rather than intended for general-purpose use. ASICs are used in a wide- range of applications, including auto emission control, environmental monitoring, and personal digital assistants (PDAs). Field-programmable gate arrays (FPGA) are the modern- day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production.

Gate - Array Design

Gate-array design is a manufacturing method in which the diffused layers, i.e. transistors and other active devices, are predefined and wafers containing such devices are held in stock prior to metallization - in other words, unconnected. The physical design process then defines the interconnections of the final device. For most ASIC manufacturers, this consists of from two to as many as nine metal layers, each metal layer running perpendicular to the one below it. Non-recurring engineering costs are much lower, as photolithographic masks are required only for the metal layers, and production cycles are much shorter, as metallization is a comparatively quick process. Gate-array ASICs are always a compromise as mapping a given design onto what a manufacturer held as a stock wafer never gives 100% utilization. Often difficulties in routing the interconnect require migration onto a larger array device with consequent increase in the piece part price. These difficulties are often a result of the layout software used to develop the interconnect.

Full – Custom Design

By contrast, full-custom ASIC design defines all the photolithographic layers of the device. Full-custom design is used for both ASIC design and for standard product design. The benefits of full-custom design usually include reduced area (and therefore recurring component cost), performance improvements, and also the ability to integrate analog components and other pre-designed - and thus fully verified - components, such as microprocessor cores that form a system-on-chip. The disadvantages of full-custom design can include increased manufacturing and design time, increased non-recurring engineering costs, more complexity in the computer-aided design (CAD) system, and a much higher skill requirement on the part of the design team.