Unit-2: Combinational logic circuits

COMBINATIONAL LOGIC CIRCUIT

• A combinational circuit consists of logic gates whose outputs at any time are determined from only the present combination of inputs.

• A combinational circuit performs an operation that can be specified logically by a set of Boolean functions. It consists of an interconnection of logic gates. Combinational logic gates react to the values of the signals at their inputs and produce the value of the output signal, transforming binary information from the given input data to a required output data.

Half adder

The most basic arithmetic operation is the addition of two binary digits. This simple addition consists of four possible elementary operations: 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, and 1 + 1 = 10.

The first three operations produce a sum of one digit, but when both augend and addend bits are equal to 1; the binary sum consists of two digits. The higher significant bit of this result is called a carry.

When the augend and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next higher order pair of significant bits.

A combinational circuit that performs the addition of two bits is called a half adder.

• This circuit needs two binary inputs and two binary outputs.

The input variables designate the augend and addend bits; the output variables produce the sum and carry. Symbols x and y are assigned to the two inputs and S (for sum) and C (for carry) to the outputs. The truth table for the half adder is listed in the below table.

Input		Output	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

C = AB

$S = G1 + G2$
$\bar{A}B + A\bar{B}$
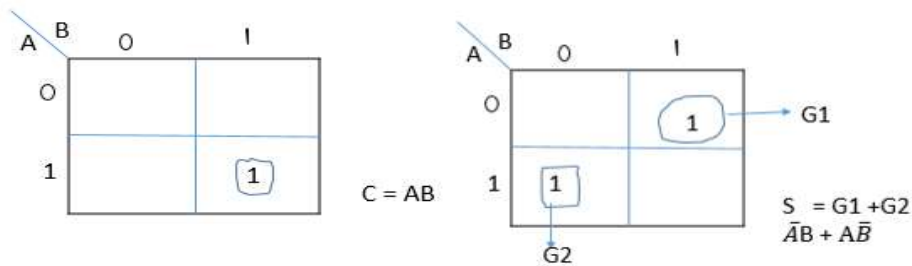
• The C output is 1 only when both inputs are 1. The S output represents the least significant bit of the sum. • The simplified Boolean functions for the two outputs can be obtained directly from the truth table.

The simplified sum-of-products expressions are   S = A'B + AB'   C = AB

• The logic diagram of the half adder implemented in sum of products is shown in the below figure. It can be also implemented with an exclusive-OR and an AND gate.

(a) $S = xy' + x'y$
    $C = xy$

(b) $S = x \oplus y$
    $C = xy$
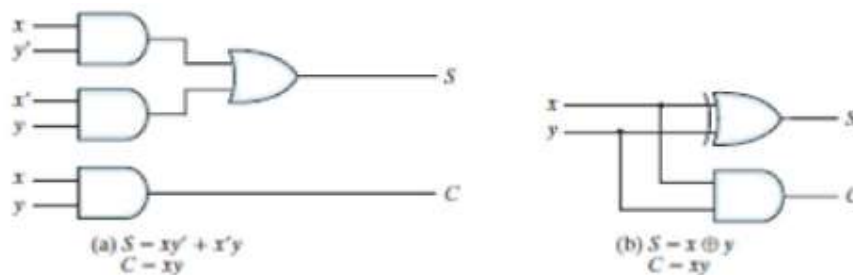
Full adder

One that performs the addition of three bits (two significant bits and a previous carry) is a full adder. The names of the circuits stem from the fact that two half adders can be employed to implement a full adder.

• A full adder is a combinational circuit that forms the arithmetic sum of three bits. • It consists of three inputs and two outputs. Two of the input variables, denoted by x and y , represent the two significant bits to be added. The third input, z , represents the carry from

the previous lower significant position. The two outputs are designated by the symbols S for sum and C for carry. The simplified expressions are
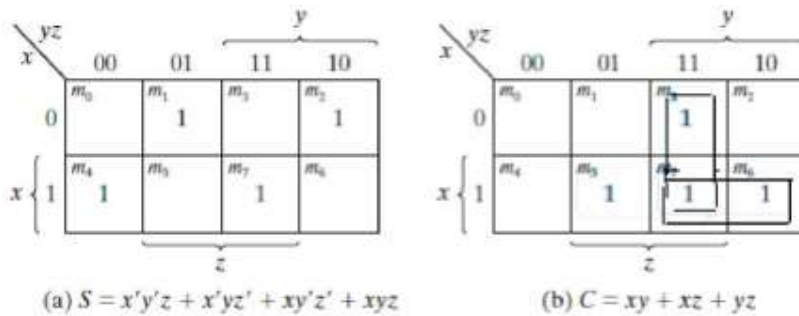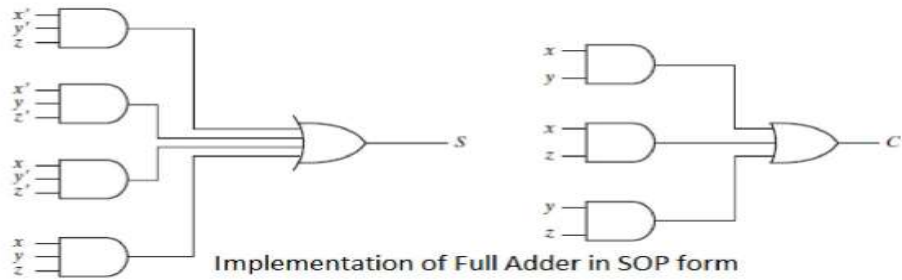
$S = x'y'z + x'yz' + xy'z' + xyz$

$C = xy + xz + yz$

• The logic diagram for the full adder implemented in sum-of-products form is shown in figure

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Truth Table

(a) $S = x'y'z + x'yz' + xy'z' + xyz$ (b) $C = xy + xz + yz$
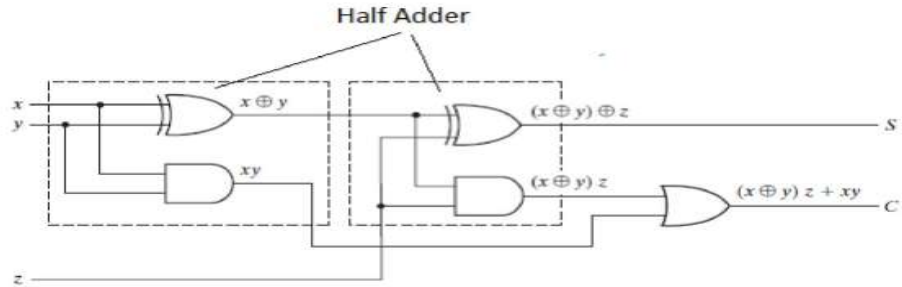
K-Map for full adder

Implementation of Full Adder in SOP form

It can also be implemented with two half adders and one OR gate as shown in the figure.
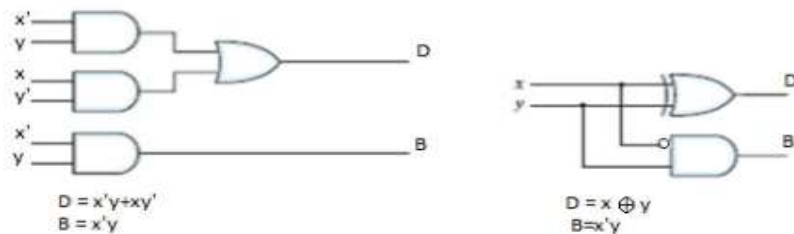

Half Subtractor

This circuit needs two binary inputs and two binary outputs. The subtraction operation is done by using the following rules as: $0 - 0 = 0$; $0 - 1 = 1$ with borrow 1; $1 - 0 = 1$; $1 - 1 = 0$

Symbols x and y are assigned to the two inputs and D (for difference) and B (for borrow) to the outputs. • The truth table for the half subtractor is listed in the below table

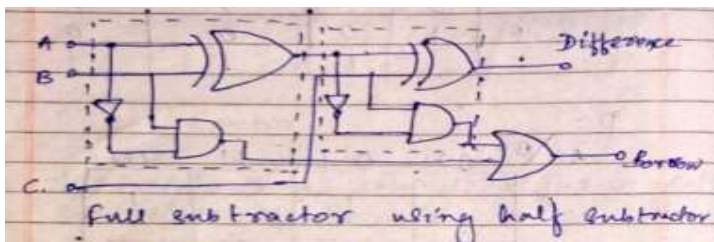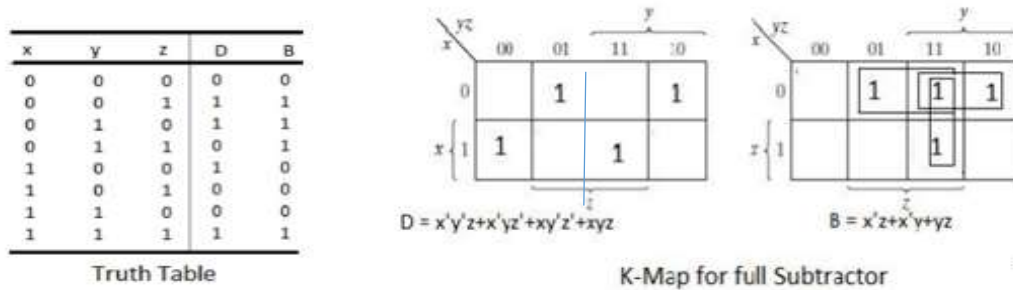| x	y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The simplified Boolean functions for the two outputs can be obtained directly from the truth table. The simplified sum-of-products expressions are $D = x'y + xy'$ and $B = x'y$

The logic diagram of the half adder implemented in sum of products is shown in the figure. It can be also implemented with an exclusive-OR and an AND gate with one inverted input.

$D = x'y+xy'$
$B = x'y$

$D = x \oplus y$
$B = x'y$

Full Subtractor

A full subtractor is a combinational circuit that forms the arithmetic subtraction operation of three bits. It consists of three inputs and two outputs. Two of the input variables, denoted by x and y , represent the two significant bits to be subtracted. The third input, z , is subtracted from the result Of the first subtraction.

x	y	z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Truth Table

$D = x'y'z + x'yz' + xy'z' + xyz$

$B = x'z + x'y + yz$

K-Map for full Subtractor


Full subtractor using half subtractor

The binary variable D gives the value of the least significant bit of the difference. The binary variable B gives the output borrow formed during the subtraction process.

Parallel Binary 4 bit adder

 A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers.

It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of the next full adder in the chain.

Addition of n-bit numbers requires a chain of n full adders or a chain of one-half adder and n-1 full adders. The interconnection of four full-adder (FA) circuits to provide a four-bit binary ripple carry adder is shown in the figure.


Four Bit Binary Adder
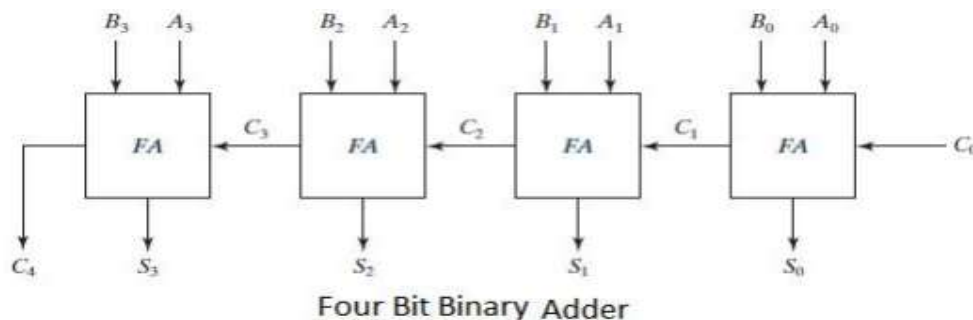
The augend bits of A and the addend bits of B are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bit. The carries are connected in a chain through the full adders. The input carry to the adder is C0, and it ripples through the full adders to the output carry C4. The S outputs generate the required sum bits.

Multiplexer (4:1)

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.

• The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected. A four-to-one-line multiplexer is shown in the below figure.


(b) Multiplexer implementation

Truth table

Logic diagram
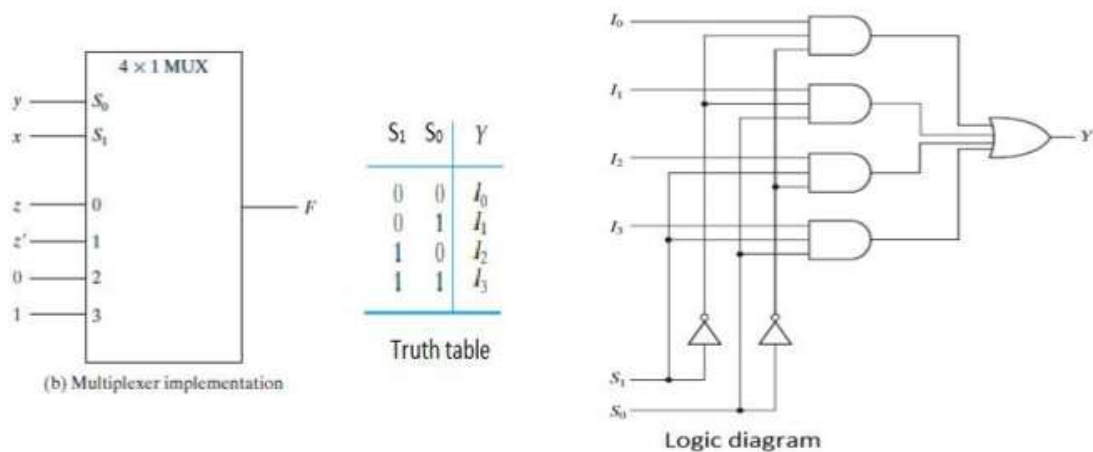
Each of the four inputs, I0 through I3, is applied to one input of an AND gate. Selection lines S1 and S0 are decoded to select a particular AND gate. The outputs of the AND gates are applied to a single OR gate that provides the one-line output.

• A multiplexer is also called a **data selector**, since it selects one of many inputs and steers the binary information to the output line.

De- multiplexer (1:4)

The data distributor, known more commonly as a Demultiplexer or "Demux" for short, is the exact opposite of the Multiplexer. • The demultiplexer takes one single input data line and then switches it to any one of a number of individual output lines one at a time. The demultiplexer converts a serial data signal at the input to a parallel data at its output lines as shown below.

Truth Table

Logic Diagram

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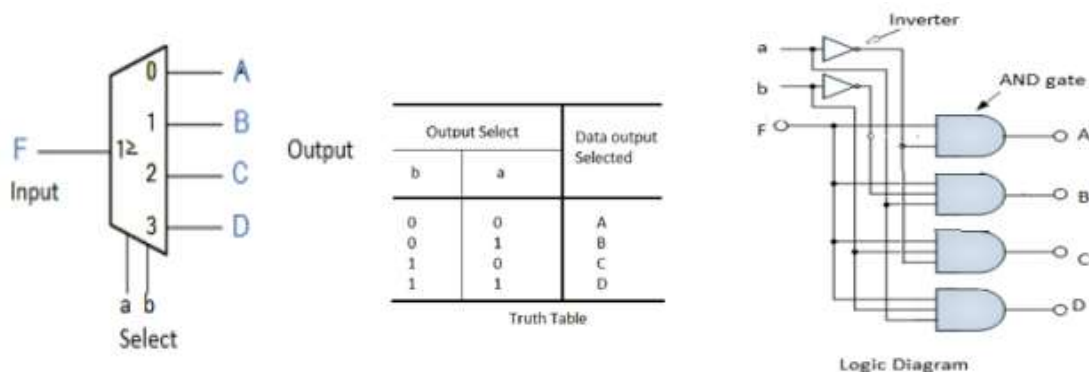
The function of the demultiplexer is to switch one common data input line to any one of the 4 output data lines A to D in our example above. As with the multiplexer the individual solid state switches are selected by the binary input address code on the output select pins "a" and "b" as shown