Memory Segmentation

Segmentation divides the main memory of a computer into logical segments to enhance execution speed, allowing the processor to efficiently fetch and execute data. The Intel 8086 microprocessor utilizes four segment registers to manage memory segments of 64KB each within a 1MB addressable space, providing advantages like improved memory management and data sharing.

The 8086 microprocessor uses four segment registers to manage memory:

- **Code Segment (CS):** Stores the executable program instructions.
- **Data Segment (DS):** Holds data required during program execution.
- **Stack Segment (SS):** Manages stack-related operations.
- **Extra Segment (ES):** Provides additional space for data overflow or auxiliary information.

Each segment is defined by a Segment Address (16-bit) and an Offset Address (16-bit). The physical address is calculated using the formula:

Physical Address = (Segment Address × 10H) + Offset Address

For example, if the segment address is 1356H and the offset address is 2E20H:
PA = (1356H × 10H) + 2E20H = 16380H

Types of Segmentation

1. Overlapping Segmentation: Two segments share some memory space, meaning their memory ranges overlap.
2. Non-Overlapping Segmentation: Segments are distinct and do not share any memory space.

Rules of Segmentation

- The starting address of a segment must be divisible by 16.
- The size of a segment can range from 16 bytes to a maximum of 64 KB.

Advantages of Memory Segmentation

- Efficient Memory Management: Simplifies handling of large memory spaces.
- Extended Addressing Capability: Allows access to 1 MB of memory using 16-bit registers.
- Logical Organization: Separates code, data, and stack for better program structure.
- Support for Large Programs: Enables programs exceeding 64 KB by dividing them into multiple segments.
- Data Sharing: Facilitates easy sharing of data between processes.

Pin Diagram 8086 Microprocessor

8086 rates into 2 modes

1) Minimum mode
2) Maximum mode

The following pins are important in both minimum & maximum mode

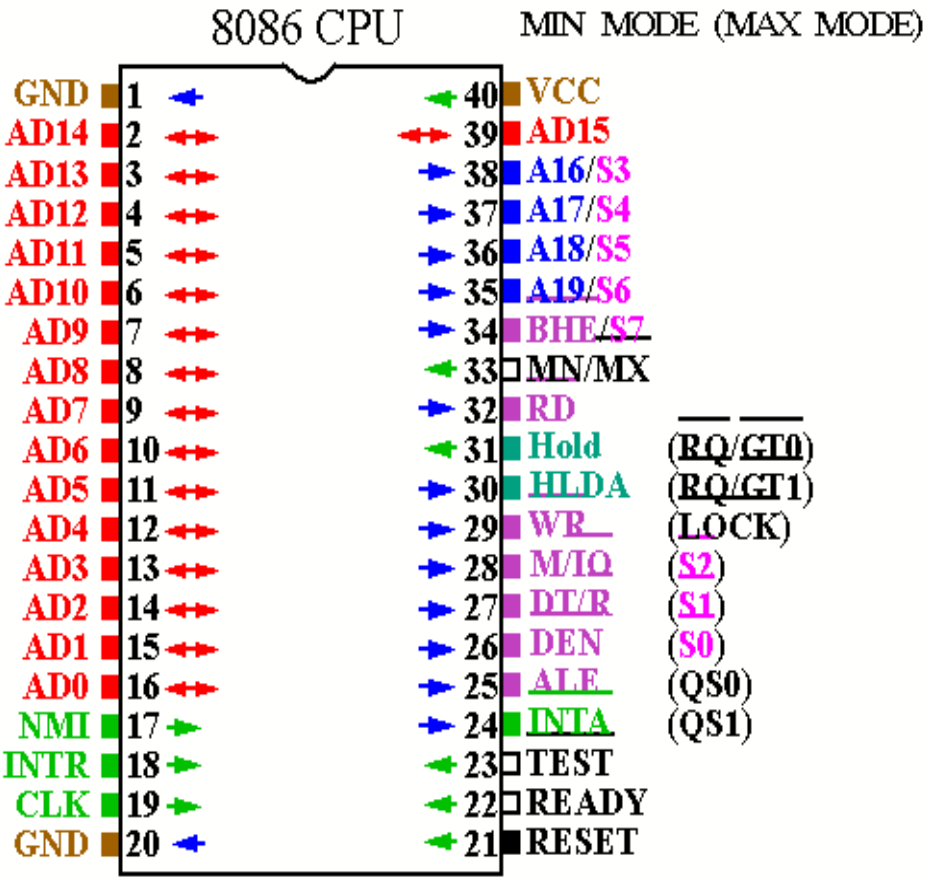
1) **CLK(pin no-19)**
   - The maximum clock frequency 5-10MHZ
   - Provides basics timing for processor & bus controller.
   - It is symmetric square wave with 33% duty cycle.

2) Vcc (pin no-40)
   - Provide +5v power supply pin

3) **GND** (pin no-1,20)
   - Ground for internal circuit

) RESET (pin no-21)
   - It is a system reset
   - When this signal goes high ,processor enter into reset state &terminate the current activity & start execution from FFFF0H
   - Active high signal -→ for at least 4 clock cycle.

5) AD0-AD15
   - These lines are multiplexed ,bi-directional address / data bus
   - 8086 has 20 bit address bus(A0-A19)
   - 16 bit data bus
   - During t1 cycle → carry lower order 16 bit address
   - T2,t3,t4 -→ carry 16 bit data
   - So AD0-AD7 lines carry lower order byte of data& AD8 –AD15 carry high order byte of data



6) A19/ s6, A18/s5, A17/s4 , A16/s3

- These lines are multiplexed address & status lines
- Upper 4 bits address sent on this lines for memory operation
- During I/O operation these lines are low
- During memory & I/O operation status information is availble on these lines in T2,T4 cycles.
- status of interrupt flag indicated by S5

S4	S3	segment Register
0	0	alternate data
0	1	stack
1	0	code
1	1	Data

7) BHE /S7 (pin no- 34) -→ bus high enable / status

During t1 state BHE signal is used to enable data on most significant half of data bus pins

D15- D8...S7 status information available during t2,t3,t4 status -→ remain high

BHE	A0	word /byte access
0	0	whole word from even address
0	1	upper byte from / to odd address
1	0	lower byte from / to even address
1	1	none

8) RD (pin no-32)

- Active low signal
- Read strobe indicates that processor is performed memory, I/O read cycle depending on s2 pin

9) Ready (pin no-22)

- When high--→ carry out it normal operation
- When low -→ freezes it's bus & enters a wait state

10) INTR (pin no-18) Interrupt request

- High level triggered interrupt request i/p
- Checked last clock to check availability of request
- If request is not occurred, processor enters interrupt acknowledge cycle

11) TEST (pin no-23)

- This i/p is examined by 8086 wait instruction
- If TEST i/p → low -→ execution continued --→ if not then processor enter /wait in idle state

12) NMI (pin no-17) Non mask able interrupt

- NMI is not mask able internally by software
- A transition from low-→ high initiates the interrupt at the end of current instruction
- It is edge triggered i/p interrupt causes type-2 interrupt

13) MN / MX

- Pin indicates the operating mode of 8086
- There are 2 modes of OS i.e maximum and minimum modes
- MN/MX -→ high 8086 operating in --→ minimum mode
- MN/MX -→ low 8086 operating in --→ maximum mode