Unit III

Introduction

- Most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form.
- Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store, or transmit the analog signal with out introducing considerable error because of superimposition of noise as in the case of amplitude modulation.
- Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise.
- The operation of any digital communication system is based upon Analog to Digital (A/D) and Digital to Analog (D/A) conversion.
- Figure 10.1, highlights a typical application with in which A/D and D/A conversion is used.

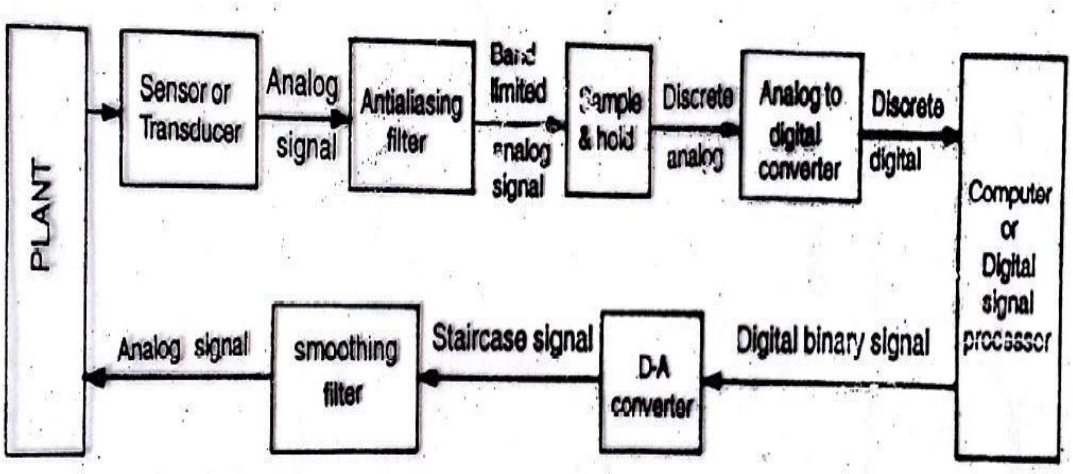

Fig. 10.1 Circuit showing application of A/D and D/A converter

- The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.
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- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.
- The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC.
- The output of a D/A converter is commonly a staircase. This staircase like output is passed through a smoothing filter to reduce the effect of quantization noise.

Applications of A/D and D/A conversion

- The scheme given in Figure 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multi meter, direct digital control, digital signal processing, microprocessor based instrumentation.

Basic DAC techniques

- The schematic of a DAC is shown in Figure 10.2.

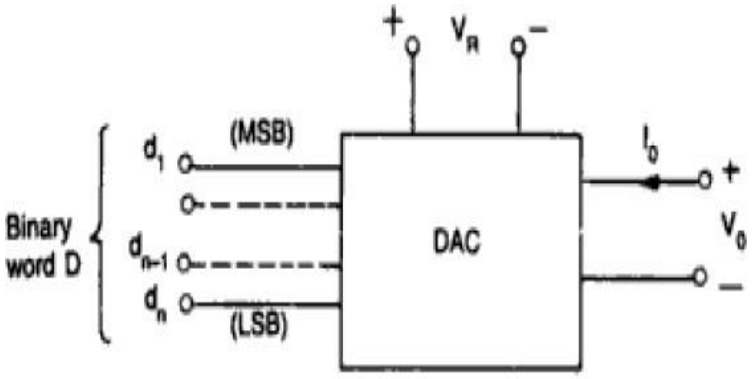


Fig. 10.2 Schematic of a DAC

- The input is an n-bit binary word D and is combined with a reference voltage vR to give an analog output signal.
- The output of a DAC can be either a voltage or current.
- For a voltage output DAC, the D/A converter is mathematically described as

Vo=K Vfs(d1 2^-1 + d2 2^-2 + d3 2^-3+ ----- +dn 2^-n) --- (1)

Where Vo = output voltage, Vfs=full scale output voltage

K = scaling factor usually adjusted to unity

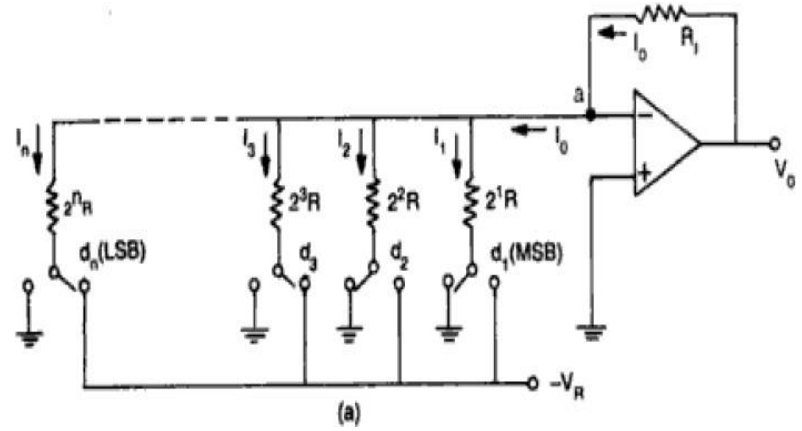
d1 d2 d3-------- dn = n-bit binary fractional word

d1 = MSB with weight of Vfs/2, dn =LSB with a weight of Vfs/2^n

- There are various ways to implement eq(1). Here we shall discuss the following resistive techniques only
    - Weighted resistor DAC
    - R-2R Ladder DAC
    - Inverted R-2R Ladder DAC

Weighted Resistor DAC:

- One of the simplest circuits shown in Figure 10.3a uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches d1, d2, d3, -----dn, controlled by Binary input word.



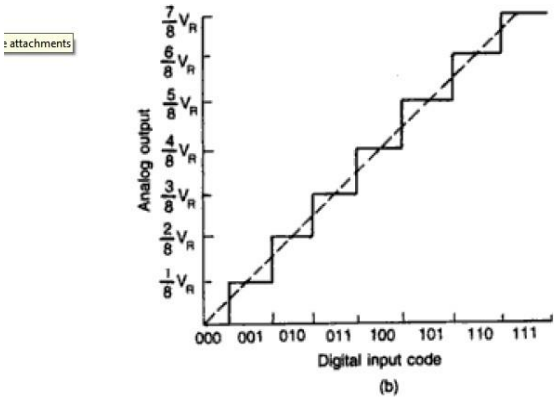


Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

- These switches are single pole double throw (SPDT) type.
- If the Binary input to a particular switch is 1, it connects the resistance to the reference voltage (-Vr). And if the input bit is zero, the switch connects the resistor to ground.
- From Figure 10.3a, the output current Io for an ideal op-amp can be written as

Io = I1 +I2 + ---------- + In

= (Vr/(2R)) d1 + (Vr/(2^2 R)) d2 + -----+(Vr/(2^n R)) dn

= Vr/R (d1 2^-1 + d2 2^-2 + --------- + dn 2^-n)

The output voltage

Vo=Io Rf=Vr Rf/R (d1 2^-1 + d2 2^-2 + ---- + dn 2^-n) – (2)

- Comparing eq(1) with eq(2), we get

if Rf = R, then K=1, and Vfs = Vr

- The circuit shown in Figure 10.3a uses a –ve reference voltage. The analog output voltage is therefore +ve staircase as shown in Figure 10.3b for a 3-bit weighted resistor DAC.
- It may be noted that
    - Although the op-amp in Figure 10.3a is connected in inverting mode, it can also be connected in non-inverting mode.
    - The op-amp is simply working as a current-to-voltage converter.
    - The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches , the reference voltage should be +5V and the output will be –ve.

Problems with Weighted Resistor DAC

- The accuracy and stability of a DAC depends up on the accuracy of the resistors and tracking of each other with temperature.
- There are, however, a number of problems associated with this type of DAC.
- One of the disadvantages of Binary weighted resistor type DAC is the wide range of resistor values required.
- It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bits increases, the range of resistance value increases.
- For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, ------ , 2^8 R. The largest resistor is 128 times the smallest one for only 8-bit DAC.
- For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5KΩ.
- The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy.
- The choice of smallest resistor value as 2.5 KΩ is reasonable, otherwise loading effect will be there.
- The difficult of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8 bits.

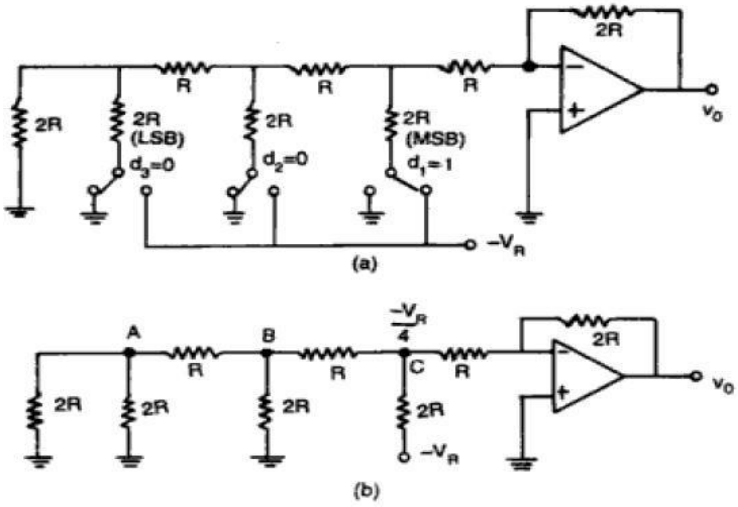
R-2R Ladder DAC:

- Wide range of resistors are required in Binary Weighted Resistor type DAC. This can be avoided by using R-2R Ladder type DAC where only two values of resistors are required.
- It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 KΩ to 10KΩ.
- For simplicity, consider a 3-bit DAC as shown in Figure 10.5a, where the switch position d1 d2 d3 corresponds to the Binary word 100.
- The circuit can be simplified to the equation form of Figure 10.5b and finally to Figure 10.5c.
- Then, voltage at node C can be easily calculated by the set procedure of network analysis as

  -Vr ((2/3) R) / (2R + (2/3)R) = -Vr/4

- The output voltage

Vo= -2R/R(-Vr/4) = Vr/2 = Vfs/2



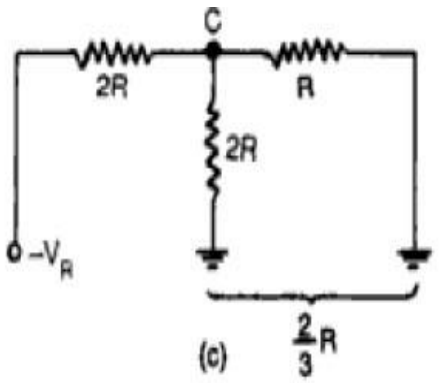


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

A/D Converters

- The block schematic of ADC shown in Figure 10.9 provides the function just opposite to that of a DAC.

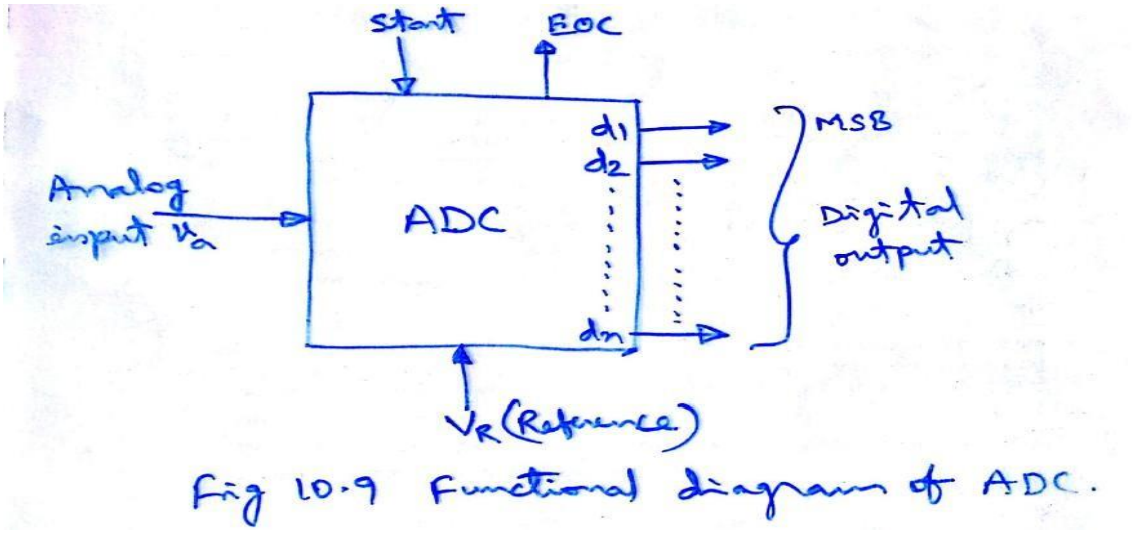


Fig 10.9 Functional diagram of ADC.

- It accepts an analog input voltage Va and produces an output binary word d1d2 ------- dn of functional value D, so that

D = d1 2^-1 + d2 2^-2 +----------+ dn 2^-n

where d1 is the MSB and dn is the LSB.

- An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and EOC (end of conversion) output to announce when the conversion is complete.
- Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.
- ADCs are classified broadly into two groups according to their conversion technique
    - Direct type ADCs
    - Integrating type ADCs
- Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes
    - Flash (comparator) type converter
    - Counter type converter
    - Tracking or servo conveter
    - Successive approximation type converter
- Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:
    - Charge balancing ADC
    - Dual slope ADC

Successive Approximation Converter

- The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods.
- For example, an 8-bit converter would require eight clock pulses to obtain a digital output. Figure 10.13 shows an 8-bit converter.

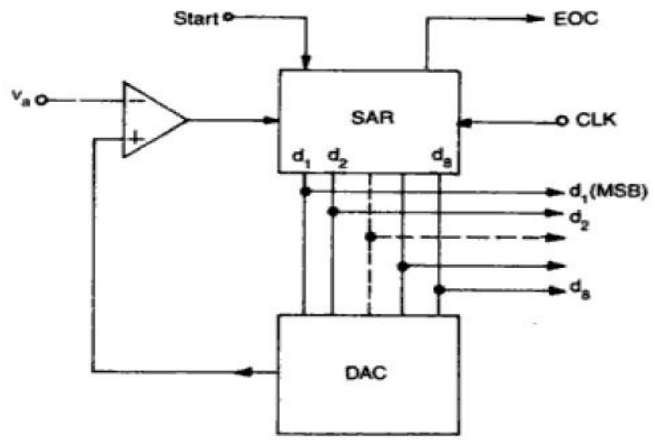


Fig. 10.13 Functional diagram of the successive approximation ADC

- The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

Circuit Operation:

- With the arrival of the START command the SAR sets the MSB d1=1, with all other bits to zero so that the trial code is 10000000.
- The output Vd of the DAC is now compared with analog input Va.
- If Va is greater than the DAC output Vd, then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.
- However, if Va is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to zero and go on to the next lower significant bit.
- This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.
- Whenever the DAC output crosses Va, the comparator changes state and this can be taken as the end of conversion (EOC) command.
- Figure 10.14a shows a typical conversion sequence and Figure 10.14b shows the associated waveforms.

Correct digital representation	*Successive approximation register output V_d at different stages in the conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

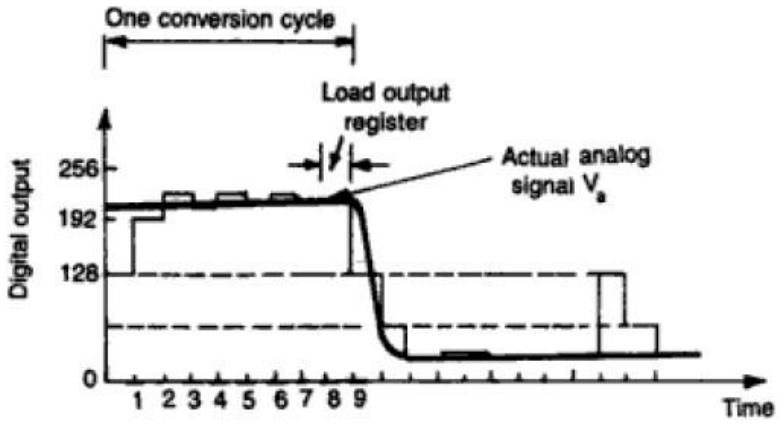


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

- It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage.
- It requires 8 pulses to establish the accurate output regardless of the value of the analog input.
- However, one additional clock pulse is used to load the output register and reinitialize the circuit.
- The AD7592 (Analog Devices Co.), a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.