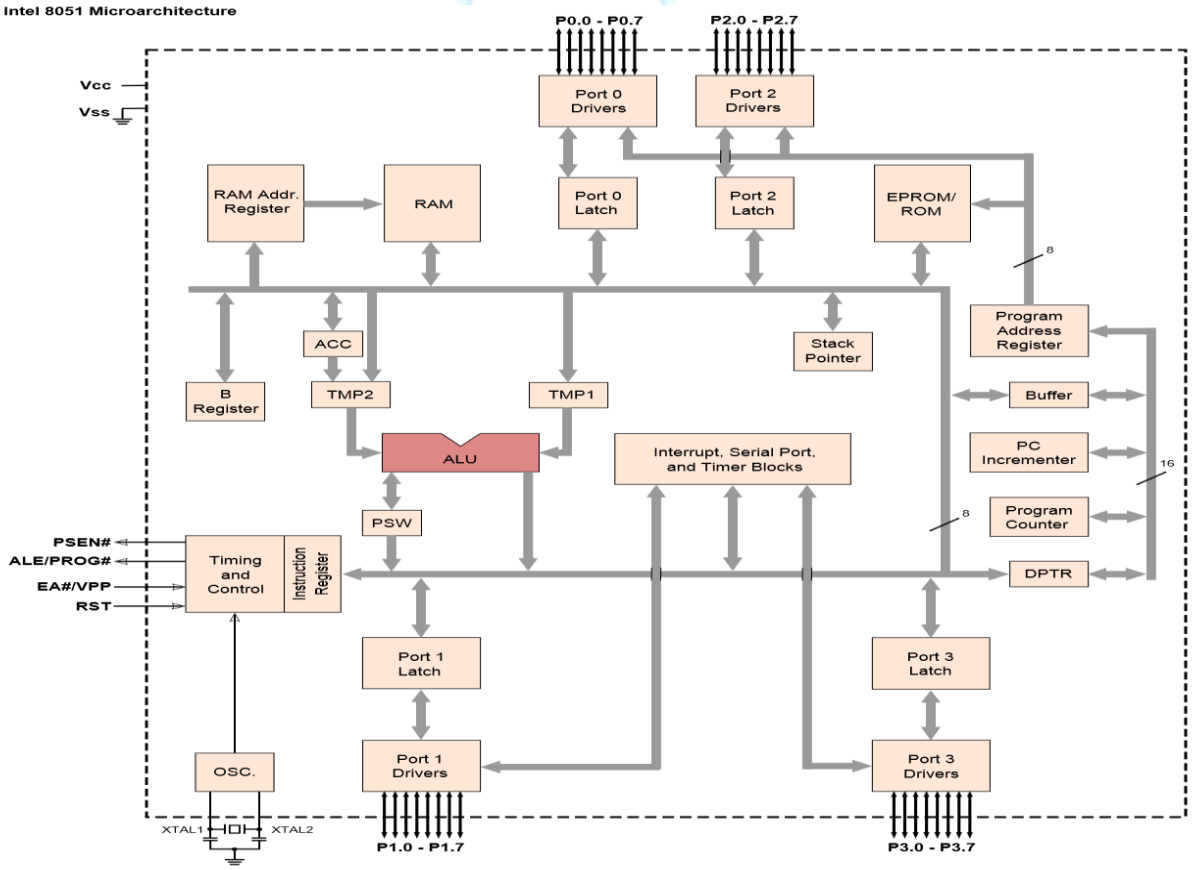
Architecture of 8051 microcontroller

The Intel 8051 contains two separate buses for both program and data. So, it has two distinctive memory spaces of 64K x 8 size for both program and data. It is based on an 8 bit central processing unit with an 8 bit accumulator and¬ another 8-bit B register as main processing blocks. Other portions of the architecture include few 8 bit and 16b it registers and 8-bit¬ memory locations. It has some amount of data RAM built in the device for internal processing. This area is used for stack operations and temporary storage of data. 8051 is supported with on-chip peripheral functions like I/O ports, Timers/¬ Counters, Serial communication port.



CENTRAL PROCESSING UNIT

The CPU is the brain of the microcontrollers expected task reading user's programs and executing the as per instructions stored there in. Its primary elements are an Accumulator (AC), Stack Pointer (SP) Program¬ Counter (PC), Program Status Word (PSW), Data Pointer (DTPR) and few more 8-bit register.

ARITHMETIC LOGIC UNIT (ALU)

The arithmetic / logic unit performs the computing functions; it includes the¬ accumulator, temporary register, arithmetic and logic circuits. The temporary register is used to hold data during an arithmetic / logic operation.¬ The result is stored in the accumulator register.

ACCUMULATOR

The accumulator register (ACC or A) act as an operand register, in case of some¬ instructions. This may either be implicit or specified in the instruction.¬ The ACC register has been allotted on address in the on-chip special function¬ register bank.

PROGRAM STATUS WORD (PSW)

This set of flags contains the status information and is considered as one of the special function registers.

D7	D6	D5	D4	D3	D2	D1	D0
PSW.7	PSW.6	PSW.5	PSW.4	PSW.3	PSW.2	PSW.1	PSW.0
CY	AC	FO	RS1	RS0	OV	---	P

Figure 3: Program Status Word (PSW)

PSW.1 : --- : User Definable Flag

PSW.2 : OV: Overflow Flag

PSW.3 : RS0: Register Bank Select Bit 0 PSW.4 : RS1: Register Bank Select Bit 1

PSW.5 : FO: Flag 0 available for general purpose

PSW.6 : AC: Auxiliary Carry Flag

PSW.7 : CY: Carry Flag

The bits PSW.3 and PSW.4 are denoted as RS0 and RS1. These bits are used to select the bank register of the RAM location.

STACK POINTER (SP)

This 8-bit register is incremented before the data is stored onto the stack using PUSH or CALL instructions. This registers contains 8-bit stack top address. The stack may be defined anywhere in the on-chip 128 byte RAM. After reset, the SP register is initialized to 07. After each write two stack operation, the 8-bit contents of the operand are stored onto the stack, after incrementing the SP register by 1. Thus if SP contains 07H, the forthcoming PUSH operation will store the date at address 08H in the internal RAM. The SP content will be incremented to 08.the 8051 stack is not a top-down data structure, like other Intel processors. This register has also been allotted on address in the especial function register bank.

DATA POINTER (DTPR)

This 16-bit register contains a higher byte (DPH) and the lower byte (DPL) of a 16-bit external data RAM address. It is accessed as a 16-bit register or two 8-bit registers as specified above. It has been allotted to two address in the special function register bank, for its two bytes DPH and DPL.

PORT 0 TO 3 LACHES AND DRIVES

This four latches and driver pairs are allotted to each of the four on-chip I/O ports. These latches have been allotted address in the especial function register bank. Using the allotted addresses, the users can communicate with these ports. These are identified as P0, P1 and P3.

SERIAL DATA BUFFER

The serial data buffer internally contains two independent registers. One of them is a transmit buffer which is necessarily a parallel–in serial–out (PISO) register. The other is called receive buffer which is a serial–in parallel–out (SIPO) register. Loading a byte to the transmit

buffer initiates serial transmission of that byte. The serial data buffer is identified as SBUF and is one of the special function register.

If a byte is written to SBUF, it initiates serial transmission and if the SBUF is read, it • reads received serial data.

TIMER REGISTER

These two 16-bit register can be accessed as the lower and upper bytes. For examples, TL0 represents the lower byte of the timing register 0, while TH0 represents the upper byte of the timing register 0. Similarly, TL1 and TH1 represent lower and higher byte of the timing register 1. All these registers an be accessed using the four addresses allotted to them which lie in the special function register (SFR) address range,i.e.80Hto FF.

CONTROL REGISTER

The special function register IP, IE, TMOD, TCON, SCON and PCON contain control and status information for interrupts, Timer / Counters and serial port. All of the registers have been allotted addresses in the special function register bank of 8051.

TIMING AND CONTROL UNIT

This unit derives all the necessary timing and control signals recovered for the internal operation of the circuit. It also derives control signals recovered for controlling the system bus.

OSCILLATOR

This circuit generates the basic timing clock signal for the operation of the circuit using crystal oscillator

INSTRUCTION REGISTER

This register decodes the Opcode of an instruction to be executed and gives information to the timing and control unit to generate necessary signal for the execution of the instruction.

EPROM and Program Address Register

This block provides an on-chip EPROM and a mechanism to internally address it. (Note that EPROM is not available in all versions of 8051)

RAM and RAM Address Register

These blocks provide internal 128 bytes of RAM and a mechanism to address it internally.

SFR (Special Function Register) Register Bank

This is a set of special function registers, which can be addressed using their respective addresses which lie in the range 80H to FFH . Finally, the interrupt, serial port and timer units control and perform their specific function under the control of the timing and control unit.