Direct Memory Access (DMA)

1. What is the primary purpose of Direct Memory Access (DMA)?

A. To increase CPU clock speed

B. To allow I/O devices to communicate directly with the CPU

C. To transfer data directly between I/O devices and main memory

D. To eliminate the need for interrupts

2. Which component manages the DMA data transfer process?

A. CPU

B. Main Memory

C. DMA Controller

D. I/O Device

3. In a DMA operation, when is the CPU involved?

A. During every data transfer

B. Only during initialization and completion

C. Only during data transfer

D. Throughout the entire process

4. DMA is mainly used to reduce

A. Cache memory size

B. CPU overhead during I/O operations

C. Power consumption

D. Memory size

5. Which of the following devices commonly uses DMA?

A. Keyboard

B. Mouse

C. Hard Disk

D. Joystick

6. Without DMA, data transfer between I/O device and memory is handled using

A. Pipelining

B. Programmed I/O

C. Interrupt-driven I/O

D. Both B and C

7. Which bus transfers the actual data during DMA operation?

A. Address Bus

B. Control Bus

C. Data Bus

D. Internal Bus

8. Which signal is used by the DMA controller to request control of the system bus?

A. Bus Grant (BG)

B. Interrupt Request (IRQ)

C. Bus Request (BR)

D. Read/Write

9. What does the CPU do after receiving a Bus Request (BR) signal?

A. Immediately releases the bus

B. Halts all processing

C. Completes the current instruction

D. Generates an interrupt

10. When the DMA controller controls the system bus, it acts as

A. Slave device

B. Interrupt handler

C. Bus master

D. Bus arbitrator

11. Which DMA register stores the starting memory address?

A. Control Register

B. Word Count Register

C. Address Register

D. Status Register

12. The number of words to be transferred in DMA is stored in

A. Address Register

B. Control Register

C. Word Count Register

D. Data Register

13. Which DMA mode transfers the entire block of data without releasing the bus?

A. Transparent Mode

B. Cycle Stealing Mode

C. Burst Mode

D. Interleaved Mode

14. In which DMA mode does the CPU lose one bus cycle per data transfer?

A. Burst Mode

B. Transparent Mode

C. Cycle Stealing Mode

D. Block Transfer Mode

15. Which DMA mode allows transfer only when the CPU is idle?

A. Burst Mode

B. Cycle Stealing Mode

C. Transparent Mode

D. Block Transfer Mode

16. Which type of DMA is used when multiple DMA devices share the same bus?

A. Single-Ended DMA

B. Dual-Ended DMA

C. Arbitrated DMA

D. Interleaved DMA

17. Interleaved DMA improves performance by

A. Transferring data in a single block

B. Alternating read and write operations

C. Blocking the CPU completely

D. Eliminating interrupts

18. Which of the following is NOT an advantage of DMA?

A. Reduced CPU involvement

B. Faster data transfer

C. Cache coherence problems

D. Improved multitasking

19. A major disadvantage of DMA is

A. Reduced data transfer speed

B. Cache coherence issues

C. Elimination of interrupts

D. Increased CPU control

20. After completing data transfer, the DMA controller

A. Shuts down the system

B. Restarts the transfer

C. Sends an interrupt to the CPU

D. Clears the memory

Part B: Answer Key

Question No.	Correct Answer
1	C
2	C
3	B
4	B
5	C
6	D
7	C
8	C
9	C
10	C
11	C
12	C
13	C
14	C
15	C
16	C
17	B
18	C
19	B
20	C