



ROHINI

COLLEGE OF ENGINEERING & TECHNOLOGY

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(AUTONOMOUS)

DC CHARACTERISTICS

Current is taken from the source into the op-amp inputs and responds differently to current and voltage due to mismatching transistor. DC output voltages are,

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

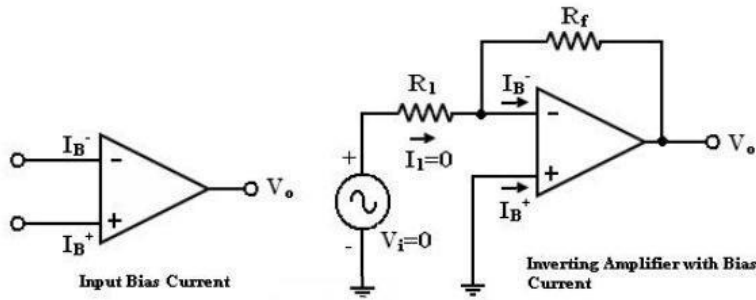
Input bias current:

The op-amp's input is differential amplifier, which may be made of BJT or FET.

In an ideal op-

amp, we assumed that no current is drawn from the input terminals; the base currents entering into the inverting and non-inverting terminals (I_B^- & I_B^+ respectively).

Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs. Manufacturers specify the input bias current I_B

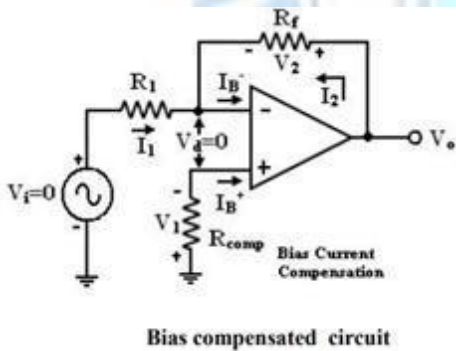


$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If input voltage $V_i=0V$. The output voltage V_o should also be ($V_o=0$) but for $I_B=500nA$ we find that the output voltage is offset by Op-amp with a $1M$ feedback resistor $V_o=500nA \times 1M=500mV$

The output is driven to $500mV$ with zero input, because of the bias currents.

In application where the signal levels are measured in nmV , this is totally unacceptable. This can be compensated by a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.



Current I_B^+ flowing through the compensating resistor R_{comp} , then by KVL we get, $-V_1+0+V_2-V_o=0$ (or)

$$V_o = V_2 - V_1 \text{-----(1)}$$

By selecting proper value of R_{comp} , V_2 can be cancelled with V_1 and the $V_o=0$. The value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp} \text{ (or)}$$

$$I_B^+ = V_1 / R_{comp} \text{-----(2)}$$

The node 'a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$.

So with $V_i = 0$ we get,

$$I_1 = V_1/R_1 \text{-----(3)}$$

$$I_2 = V_2/R_f \quad (4)$$

For compensation, V_o should equal to zero ($V_o = 0, V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$$I_2 = V_1/R_f \text{----->(5)}$$

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1 + R_f)/R_1 R_f \text{-----(5)}$$

Assume $I_B^- = I_B^+$ and using equation (2) & (5) we get

$$V_1 (R_1 + R_f)/R_1 R_f = V_1/R_{comp}$$

$$R_{comp} = R_1 \parallel R_f \text{----- (6)}$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f .

Input offset current:

i. Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. ii.

Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^- . This difference is called the offset current

$$|I_{os}| = I_B^+ - I_B^- \text{-----(7)}$$

Offset current I_{os} for BJT op-amp is 200 nA and for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$$V_1 = I_B^+ R_{comp} \text{----- (11)}$$

$$\text{And } I_1 = V_1/R_1 \text{----- (12)}$$

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - (I_B^+ \frac{R_{comp}}{R_1})$$

Output voltage =

$$\text{Again } V_o = I_2 R_f - V_1$$

$$V_o = I_2 R_f - I_B + R_{comp}$$

$$V_o = 1\text{M}\Omega \times 200\text{nA}$$

$$V_o = 200\text{mV with } V_i = 0$$

Equation(16) the offset current can be minimized by keeping feedback resistances small.

- Unfortunately to obtain high input impedance, R_1 must be kept large.
- R_1 large, the feedback resistor R_f must also be high. So to obtain reasonable gain.

The T-

feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (indotted line).

The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

$$R_f = \frac{R_t^2 + 2R_t R_s}{R_s}$$

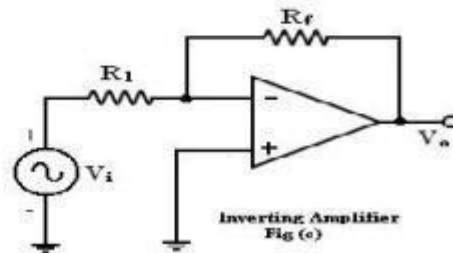
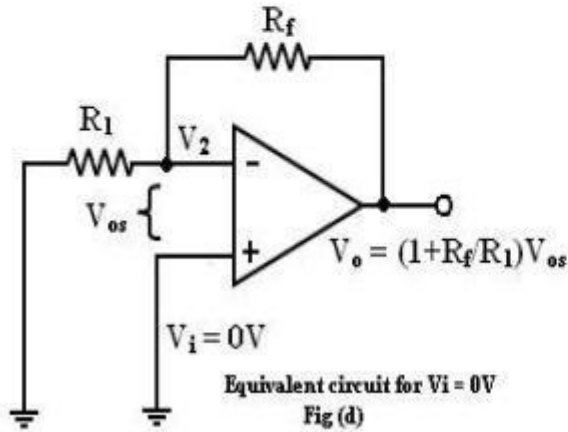
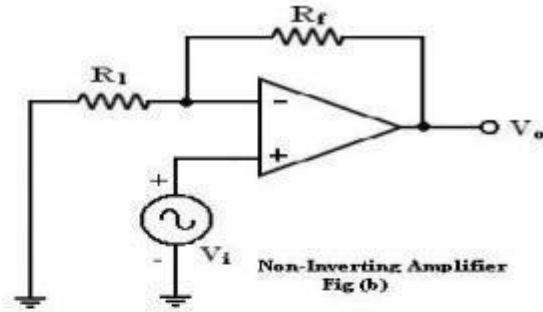
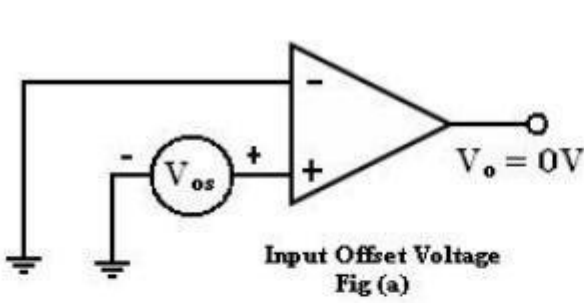
To design T-network first pick $R_t \ll R_f/2$ and calculate

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

Input offset voltage:

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [$V_o \neq 0$ with $V_i = 0$]. This is due to un avoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (V_o) = 0.

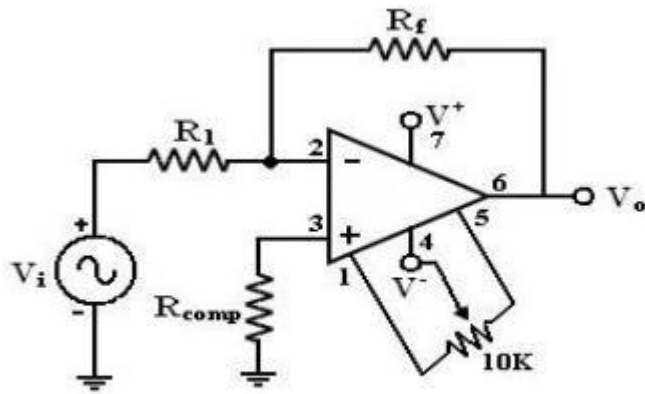
This voltage is called input offset voltage V_{os} . This is the voltage required to be applied at the input for making output voltage to zero ($V_o = 0$).



Let us determine the V_o on the output of inverting and non-inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone (V_{os}). This is because I_B and V_{os} could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many opamps provide offset compensation pin to nullify the offset voltage. A 10K potentiometer is placed across offset null pins 1 & 5. The wiper is connected to the negative supply at pin 4. The position of the wiper is adjusted to nullify the offset voltage.



Compensation circuit for offset voltage

When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

With R_{comp} , the total output offset

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

Thermal drift:

Bias current, offset current, and offset voltage change with temperature. A circuit can be fully null at 25°C but may not remain so when the temperature rises to 35°C. This is called drift. Offset current drift is expressed in nA/°C. These indicate the change in offset for each degree Celsius change in temperature.