ROHINI
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
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KANYAKUMARI, TAMIL NADU

24EC302 DIGITAL LOGIC CIRCUITS AND DESIGN

INNOVATIVE TEACHING METHOD

I YEAR AI DS II SEMESTER

ACTIVITY SHEET

Activity 1

Aim

To understand the relationship between state tables, state diagrams, and ASM charts.

State Table

Present State	Input X	Next State	Output Z
A	**0**	**A**	**0**
A	**1**	**B**	**0**
B	**0**	**C**	**1**
B	**1**	**A**	**0**
C	**0**	**C**	**1**
C	**1**	**B**	**0**

Activity

1. Draw the **state diagram**
2. Convert the state diagram into an **ASM chart**
3. Identify:
    - Moore or Mealy machine?
    - Number of decision boxes.

Activity 2

State Minimization (Equivalent States)

Aim

To minimize states by identifying equivalent states.

State	Input 0	Input 1
A	B	C
B	D	A

State	Input 0	Input 1
C	B	C
D	D	A

Activity

1. Identify equivalent states using comparison.
2. Eliminate redundant states.
3. Draw: Original state diagram and Minimized state diagram.
4. Count the number of states before and after minimization.

Activity 3

Hazard Identification in Asynchronous Circuits

Aim

To identify static and dynamic hazards.

Given Logic Expression:

$$F=A'B+AB'$$

Activity

1. Draw the logic circuit.
2. Identify if a hazard exists.
3. Sketch the timing diagram.
4. Suggest a hazard-free modification.