1.4 MEMORY STRUCTURE IN 8085 PROCESSOR

Memory Structure and Its Requirements:

- Read/Write memory is a group of registers to store binary information. Fig 1.4.1 shows a typical R/W memory chip; it has "2n = M" registers (where n= no. of address lines) and each can store N no. of bits.
- It has N no. of bidirectional (or separate input-output) data lines.
- It also has one Chip select (CS), and two control lines Read (RD) to enable the output buffer and Write (WR) to enable the input buffer.
- Figure. 1.4.1 shows the logic diagram of typical EPROM (Erasable Programmable Read Only memory) Memory with "2n = M" registers (where n= no. of address lines).
- It has "n" no. of address lines, one Chip select (CS) and one Read (RD).
- This memory chip must be programmed before it can be used as Read-Only memory.

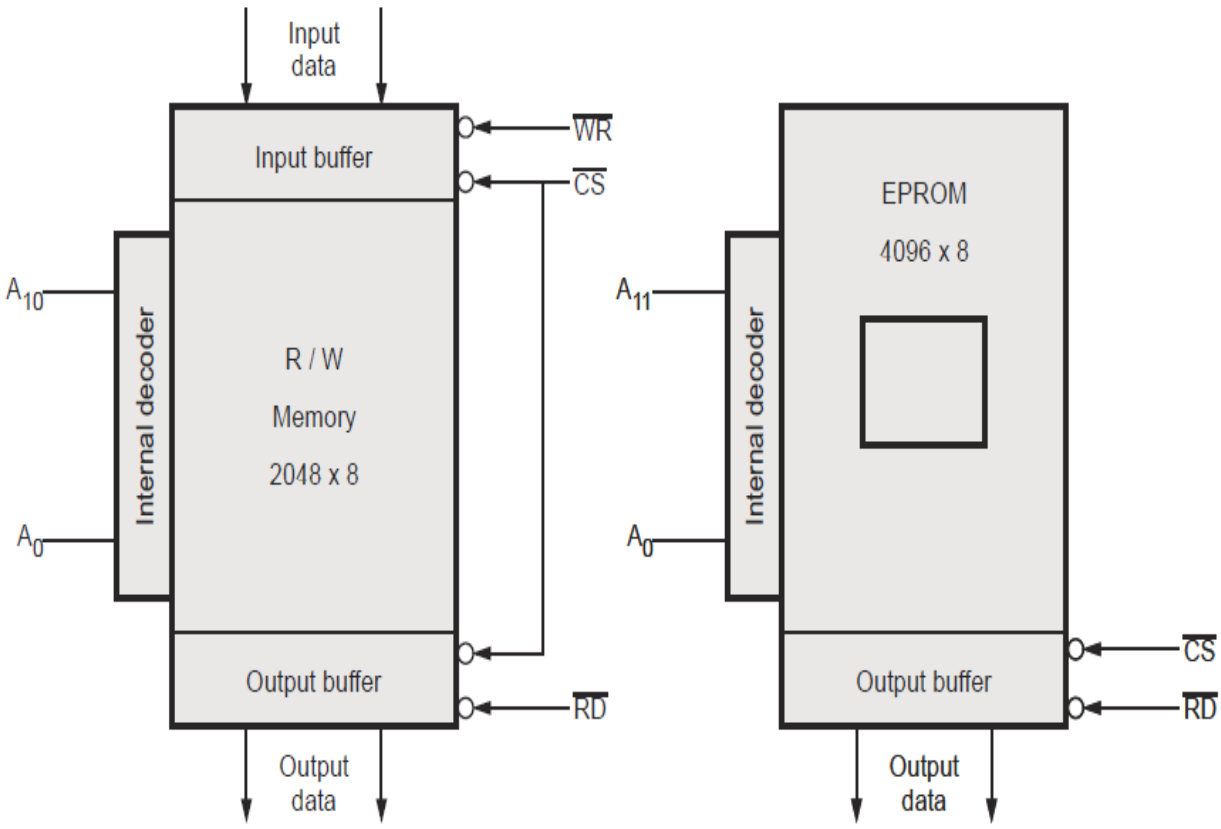

Figure 1.4.1 logic diagram of typical EPROM

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-91]

The 8085 microprocessor uses a16-bit wide address bus for addressing memories and I/O devices. Using 16-bit wide address bus it can access 216 = 64K bytes of memory and I/O devices. The 64K addresses are to be assigned to memories and I/O devices for their addressing. There are two schemes for the allocation of addresses to memories and input / output devices:

1. Memory mapped I/O scheme.
2. I/O mapped I/O scheme.

Memory mapped I/O scheme:

- In memory mapped I/O scheme there is only one address space.
- Address space is defined as the set of all possible addresses that microprocessor can generate.
- Some addresses are assigned to memories and some addresses to I/O devices.
- An I/O device is also treated as memory location and one address is assign to it.
- Suppose that memory locations are assigned the addresses 2000 H to 24FF H then each one address is assign to each memory location. The addresses for I/O devices are different from the addresses which have been assigned to memories.
- The addresses which have not been assigned to memories can be assigned to each I/O device.
- In this scheme all the data transfer instructions of the microprocessor can be valid for data transfer from the memory location or I/O device whose address is in H-L pair.

I/O mapped I/O scheme:

- In this scheme the addresses assigned to memory location can also be assigned to I/O devices.
- Since the same address may be assigned to memory location or an I/O device, the microprocessor must issue a signal to distinguish whether the address on the address bus is for a memory location or an I/O device.
- The 8085 issues an IO/M signal for this purpose.
- Two extra instructions IN and OUT are used to address I/O devices.

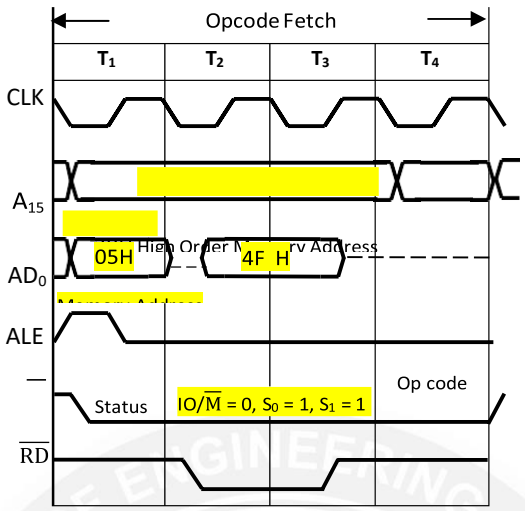

Figure 1.4.2 Timing Diagram: Transfer of Byte from Memory to Microprocessor

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-66]

- Figure 1.4.2 shows the timing diagram of how a data byte is transferred from memory to the microprocessor from which the need for demultiplexing the bus AD0-AD7 becomes easier to understand.
- This figure shows that the address on the high order bus (20H) remains on the bus for three clock periods.
- However, the low order address (05H) is lost after the first clock period.
- This address needs to be latched and used for identifying the memory address.
- If the bus AD7-AD0 is used to identify the memory location (2005H), the address will change to 204FH after the first clock period.
- Figure. 1.4.2 shows a schematic that uses a latch and the ALE signal to demultiplex the bus. The bus AD7-AD0 is connected as input to latch 74LS373.
- The ALE signal is connected to Enable (G) pin of the Latch, and the Output control (OC) signal of the latch is grounded.
- Figure 1.4.2 shows that the ALE goes high during T1. When the ALE is high, the latch is transparent; that means output changes according to the input data.
- During T1 output of the latch is 05H.
- When ALE goes low, the data byte 05H is latched until the next ALE, and the output of the latch represents the low-order address bus A7-A0 after the latching operation.

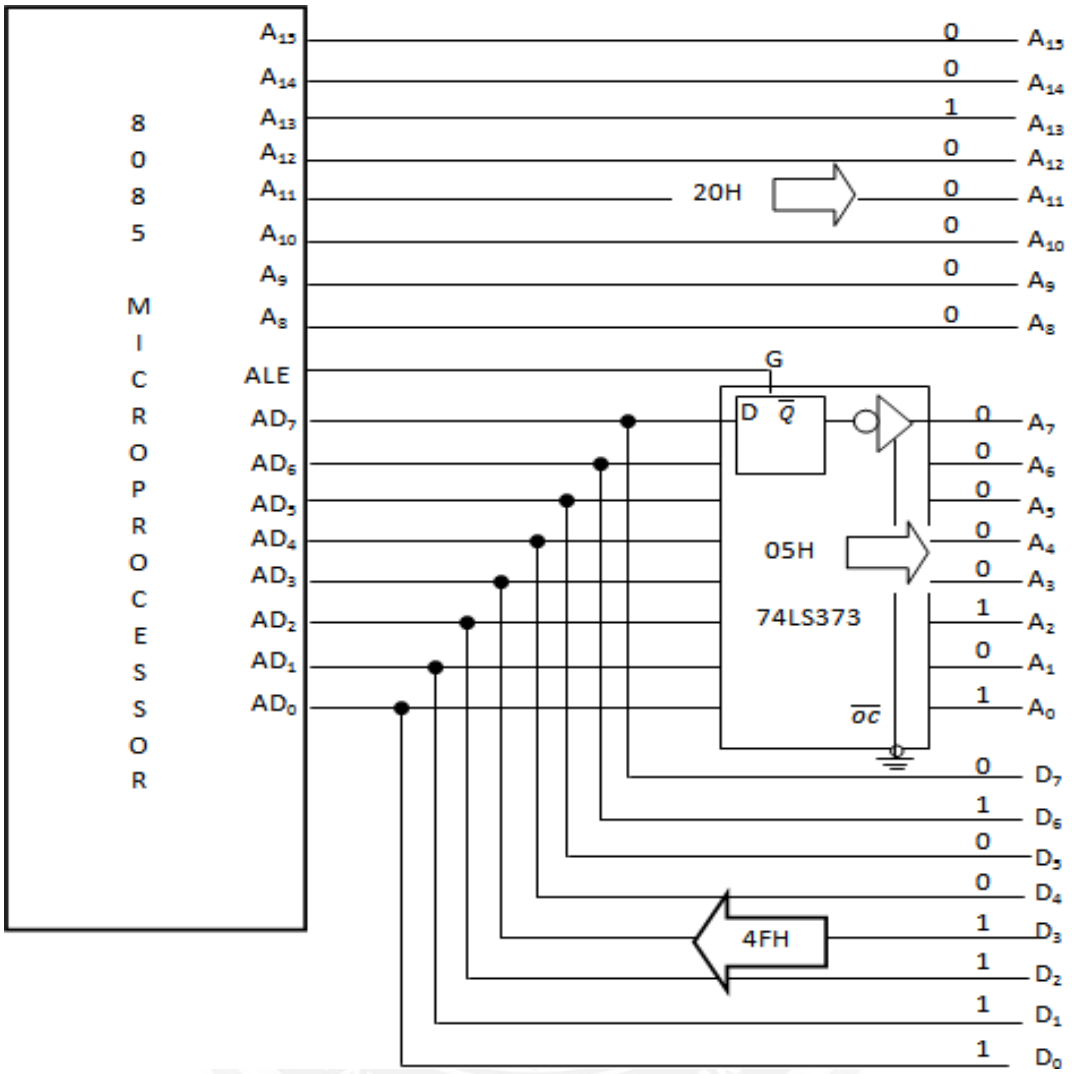

Figure 1.4.3 Schematic of Latching Low-Order Address Bus

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-82]

Generating Control Signals:

- Figure 1.4.3 shows the RD (Read) as a control signal. Because this signal is used both for reading memory and for reading an input device, it is necessary to generate two different Read signals: one for memory and another for input. Similarly, two separate Write signals must be generated.
- This signal is Indeed with RD and WR signals by using the 74LS32 quadruple two-input OR gates, as shown in Figure 1.4.3.
- When both the input goes low , the outputs of the gates go low and generate MEMR (memory Read) and MEMW (memory Write) control Signals.

- When IO/M goes high, it indicates the peripheral I/O operation. The table shows that this signal is complemented and ANDed with RD and WR signals to generate IOR (I/O Read) and IOW (I/O Write) control Signals.

$IO/\overline{M}$	$\overline{RD}$	$\overline{WR}$	**Control Signal**
0	0	1	Memory read
0	1	0	Memory write
1	0	1	I/O read
1	1	0	I/O write

Address Decoding:

- The address of a memory location is sent out by the microprocessor. The corresponding memory chip or I/O device is selected by a decoding circuit.
- The decoding task can be performed by a decoder, a comparator, a bipolar PROM or PLA (Programmed logic array).
- For memory interfacing we can use Decoder IC 74LS138 which has G1, G2A and G2B enable signals.
- To enable 74LS138, G1 should be high, and G2A and G2B should be low. Also, 74LS138 has three select lines A, B & C. By applying proper logic to select ines any one of the output cab be selected.
- Where, 74LS138 has Y0, Y1, …. Y7 output lines. An output lines goes low when it is selected. Other output lines remain high. Thus as shown in Table1.1 (Truth table for 74LS138), when G1 is low or G2A is high or G2B is high, all output lines become high.
- Thus 74LS138 acts as decoder only when G1 is high, and G2A and G2B are low.

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	**L**	H	H	H	H	H	H	H
H	L	L	L	L	H	H	**L**	H	H	H	H	H	H
H	L	L	L	H	L	H	H	**L**	H	H	H	H	H
H	L	L	L	H	H	H	H	H	**L**	H	H	H	H
H	L	L	H	L	L	H	H	H	H	**L**	H	H	H
H	L	L	H	L	H	H	H	H	H	H	**L**	H	H
H	L	L	H	H	L	H	H	H	H	H	H	**L**	H
H	L	L	H	H	H	H	H	H	H	H	H	H	**L**

Following fig shows the simple interfacing of 8K memory with 8085

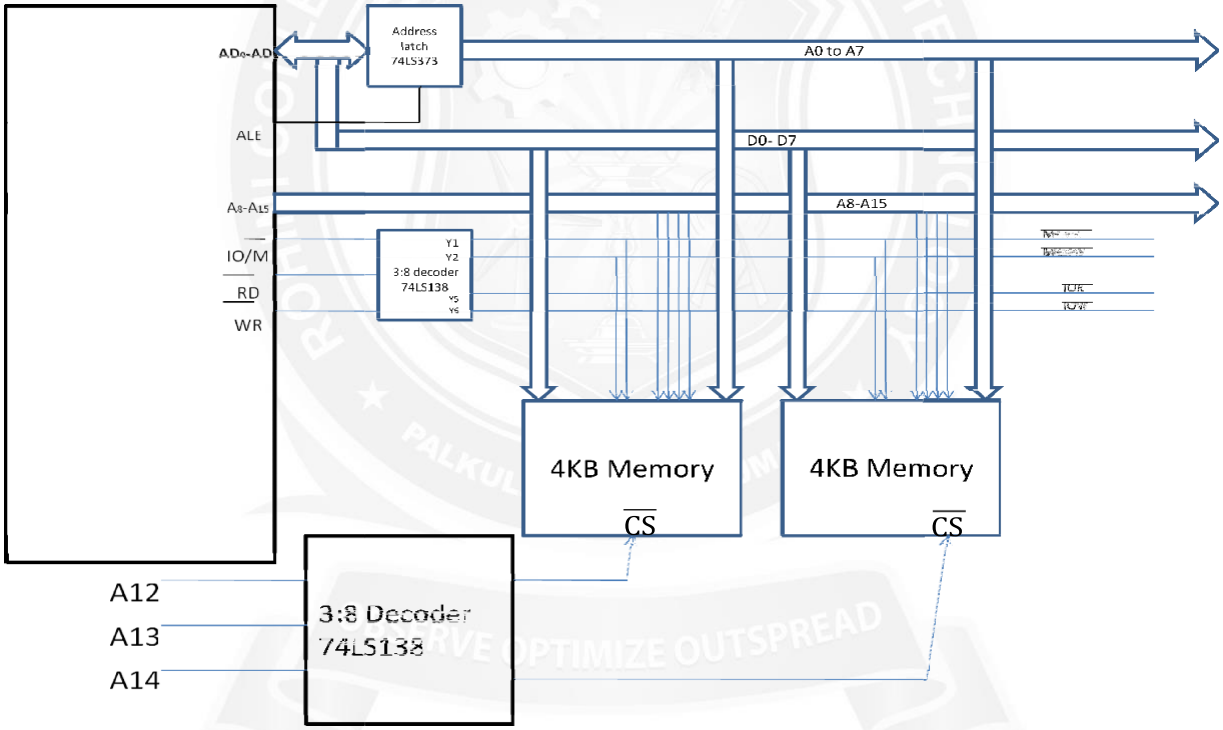

Figure 1.4.4 simple interfacing of 8K memory with 8085

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-82]