1.3 PINOUTS IN 8085 MICROPROCESSOR

The description of various pins is as follows,

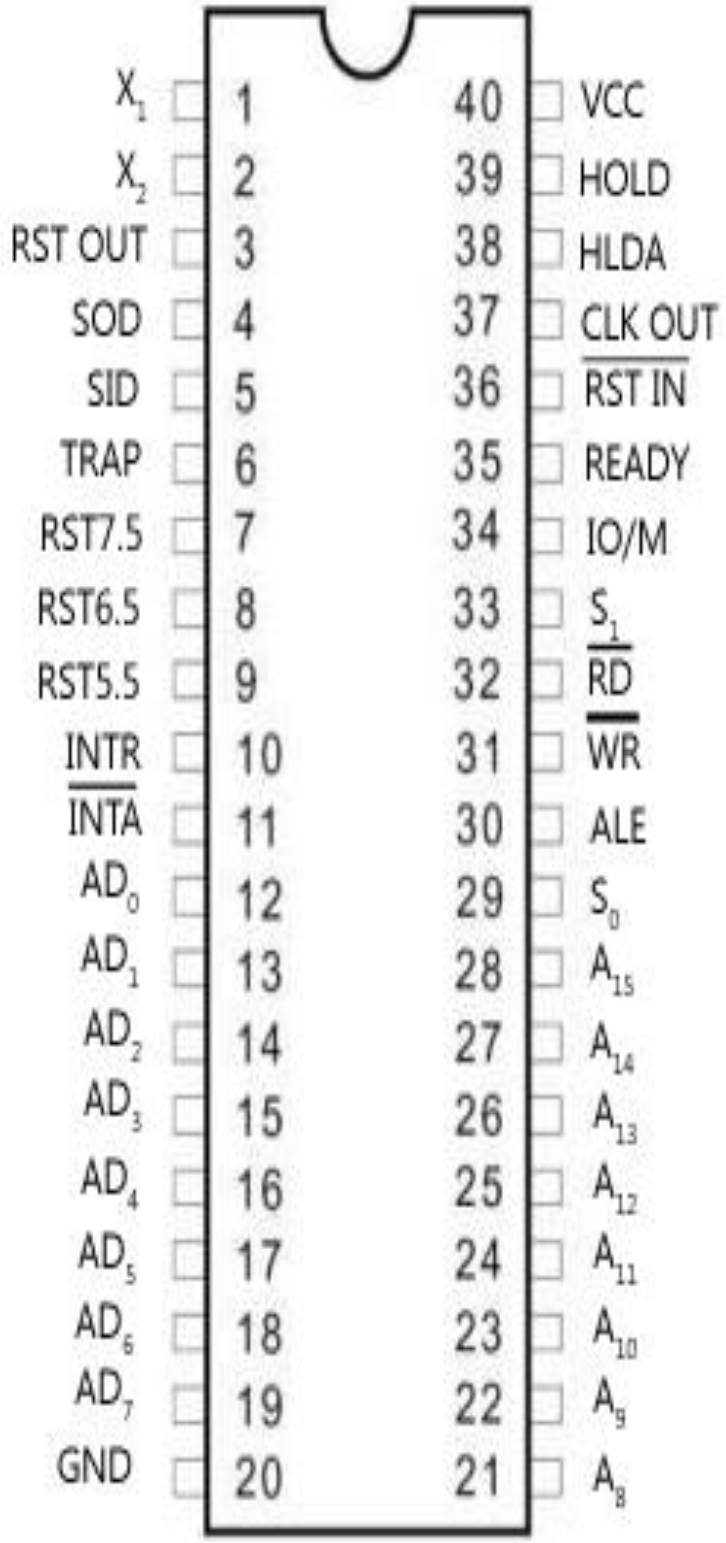

Figure 1.3.1 Pinouts of 8085 processor

[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page-41]

A8 – A15:

- These are the output lines
- These are the parallel address lines called as Address bus and are used for the most significant bits of the memory address or 8 bits of I/O address.

AD0 – AD7:

- Input / Output lines
- These are time multiplexed address/data bus i.e. they serve dual purpose.
- They are used for the least significant 8 bits of memory address or I/O address during the first clock cycle of a machine cycle.
- Again they are used for data during second and third clock cycles.

ALE:

- It is an output pin.
- It is an address latch enable signal.
- It goes high during first clock cycle of a machine cycle and enables the lower 8 bits of the address to be latched either in to the memory or external latch.

IO/M:

- It is an output status signal which distinguishes whether the address is for memory or I/O.
- When it goes high the address on the address bus is for an I/O device.
- When it goes low the address on the address bus is for a memory location.

S0, S1:

- These are the output status signals sent by the microprocessor to distinguish the various types of operations as given below.
- Status codes for 8085,

S_1	S_0	Operation
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

RD:

- It is an output control signal.

- It controls the READ operation.
- When it goes low selected memory or I/O device is read.

WR:

- It is an output control signal.
- It controls the WRITE operation.
- When it goes low data on the data bus is written into the selected memory or I/O location.

READY: (input)

- It is used by the microprocessor to sense whether a peripheral is ready to transfer data or not.
- A slow peripheral may be connected to the microprocessor through READY line.
- If READY is high peripheral is ready.
- If it is low microprocessor waits till it goes high.

HOLD (input):

- It indicates that another device is requesting for the use of address and data bus.
- After receiving the HOLD request microprocessor handover the controls of buses to that devices as soon as current machine cycle is completed. Internal processing may continue.
- The processor regains the control over the buses after removal of HOLD signal.
- When hold is acknowledged, address bus, data bus, RD, WR, and IO/M are tri-stated.
- HOLD is sampled in T2 Clock Cycle.

HLDA (output):

- It is signal for HOLD acknowledgement.
- It indicates that the HOLD request has been received.
- After removal of a HOLD request the HLDA goes low.
- The CPU takes over the buses half clock cycle after the HLDA goes low.

INTR (input):

- It is an interrupt request signal.
- Among interrupts it has lowest priority.

- When it goes high the program counter does not increment its content.
- The microprocessor suspends its normal sequence of instructions.
- After completing the instruction at hand it attends the interrupting device.
- The INTR line is sampled in the last state of the last machine cycle of an instruction.
- The INTR is enabled or disabled by software.
- An interrupt is used by I/O device to transfer data to microprocessor without wasting time.
- If CPU is in HOLD state or interrupt enable flip-flop is reset, an interrupt request is not honored.

INTA: (output)

- It is an interrupt acknowledgement sent by the microprocessor after INTR is received.

RST 5.5, 6.5 and TRAP: (inputs)

- These are the interrupts.
- When an interrupt is recognized the next instruction is executed from a fixed location in the memory as given below:

Interrupt	Vectored location
TRAP	0024
RST5.5	002C
RST6.5	0034
RST7.5	003C

- RST 7.5, RST6.5 and RST 5.5 are the restart interrupts. They cause an internal restart to be automatically inserted, each them has programmable mask.
- The TRAP has highest priority among the interrupts and it is non-maskable interrupt.

- The order of priority of interrupts is as follows:

  TRAP (Highest Priority)

  RST7.5

  RST6.5 RST5.5

  INTR (Lowest Priority)

RESET IN: (input)

- It resets the program counter to 0.
- It also resets interrupt enable and HLDA flip-flops.
- It does not affect any other flag or register except the instruction register.
- The CPU is held in reset condition as long as RESET is applied.

RESET OUT: (output)

- It indicates that the CPU is being reset.

X1, X2: (input)

- These are terminals connected to an external crystal oscillator which drives an internal circuitry of the microprocessor to produce a suitable clock for the operation of microprocessor.

CLK: (output)

- It is a clock output for user, which can be used for other digital ICs. Its frequency is same at which microprocessor operates.

SID: (input)

- It is a data line for serial input.
- The data on this line is loaded into the 7th nit of the accumulator when RIM instruction is executed.

SOD: (output)

- It is a data line for serial output. The 7th bit of the accumulator is output on SOD line when SIM instruction is executed.

Vcc:

- +5 volts supply.

Vss:

- Ground reference.