2.5 SINGLE-PHASE CURRENT SOURCE INVERTER

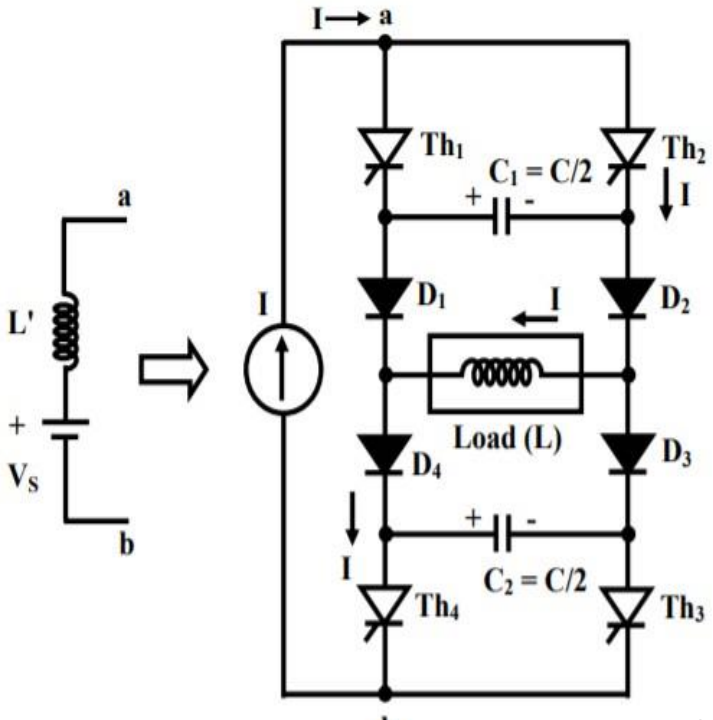

Figure 2.5.1 Single phase current source inverter (CSI)

[Source: "Power Electronics" *by* P.S.Bimbra*,* Khanna Publishers *Page: 364]*

The circuit of a Single-phase Current Source Inverter (CSI) is shown in Fig. The type of operation is termed as Auto-Sequential Commutated Inverter (ASCI). A constant current source is assumed here, which may be realized by using an inductance of suitable value, which must be high, in series with the current limited dc voltage source. The thyristor pairs, Th1 & Th3, and Th2 & Th4, are alternatively turned ON to obtain a nearly square wave current waveform. Two commutating capacitors − C1 in the upper half, and C2 in the lower half, are used. Four diodes, D1–D4 are connected in series with each thyristor to prevent the commutating capacitors from discharging into the load. The output frequency of the inverter is controlled in the usual way, i.e., by varying the half time period, (T/2), at which the thyristors in pair are triggered by pulses being fed to the

respective gates by the control circuit, to turn them ON, as can be observed from the waveforms. The inductance (L) is taken as the load in this case, the reason(s) for which need not be stated, being well known. The operation is explained by two modes.

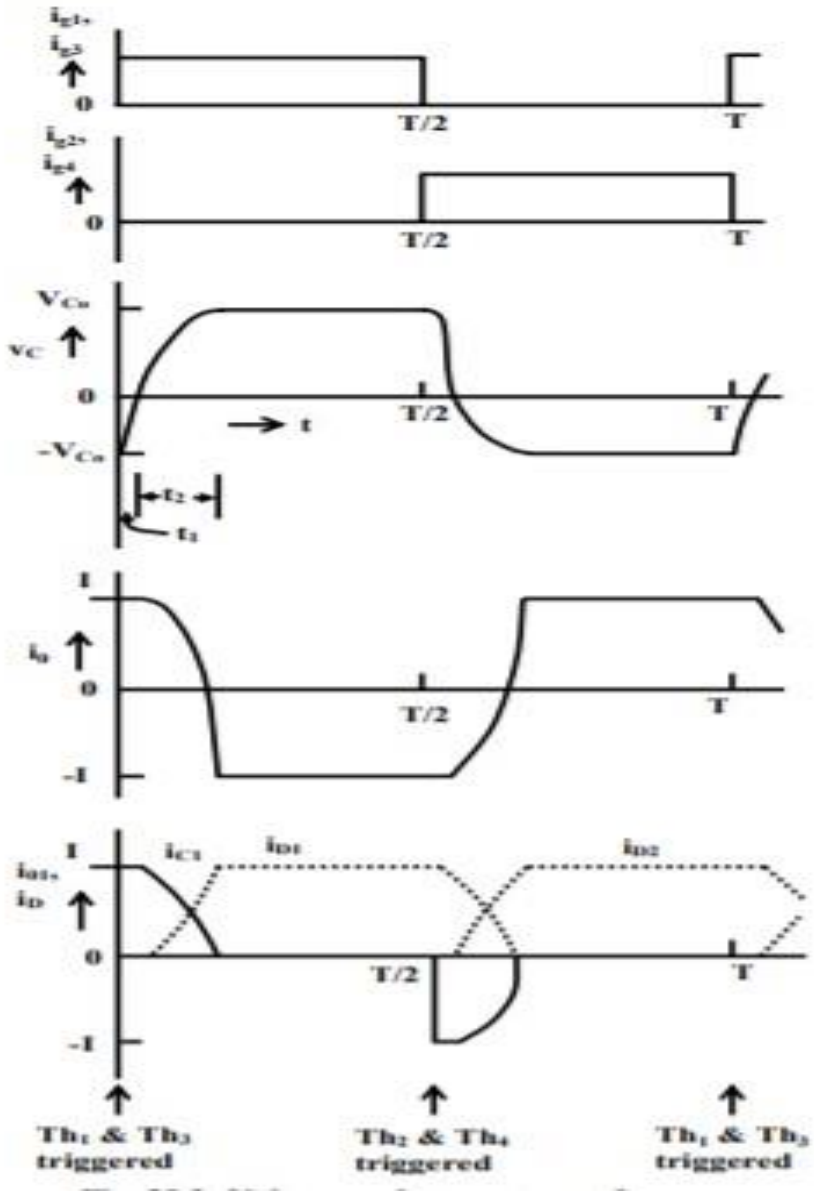

Figure 2.5.2 wave forms of Single phase current source inverter

[Source: "Power Electronics" *by* P.S.Bimbra, Khanna Publishers *Page: 365]*

Mode I: The circuit for this mode is shown in Fig. The following are the assumptions. Starting from the instant ,t= 0 , the thyristor pair, Th 2 & Th4, is conducting (ON), and the current (I) flows through the path, Th2, D2, load (L), D4, Th4, and source, I. The commutating capacitors are initially charged equally with the polarity as given, i.e., . This mans that both capacitors have right hand plate positive and left hand plate negative. If two capacitors are not charged initially, they have to pre-charged.

At time, t = 0, thyristor pair, Th1 & Th3, is triggered by pulses at the gates. The conducting thyristor pair, Th2 & Th4, is turned OFF by application of reverse capacitor voltages. Now, thyristor pair, Th1 & Th3, conducts current (I). The current path is through Th1, C1, D2, L, D4,C2, Th3, and source, I. Both capacitors will now begin charging linearly from –Vco by the constant current, I. The diodes, D2& D4, remain reverse biased initially. As the capacitor gets charged, the voltage vD1 across D1, increases linearly. At some time, say t1, the reverse bias across D1 becomes zero (0), the diode, D1.starts conducting. This means that the voltages across C1 & C2, varies linearly from –Vco to zero in time, t1. Mode I ends, whent=t1, and vc= 0 . Note that t1 is the circuit turn-off time for the thyristors.

Mode II: The circuit for this mode is shown in Fig. 39.4a. Diodes, D2 & D4, are already conducting, but at t = t1 , diodes, D1 & D3, get forward biased, and start conducting. Thus, at the end of time t1, all four diodes, D1–D4 conduct. As a result, the commutating capacitors now get connected in parallel with the load (L).At the end of the process, constant current flows in the path, Th1, D1, load (L), D3, Th3, and source, I. This continues till the

next commutation process is initiated by the triggering of the thyristor pair, Th2 & Th4.