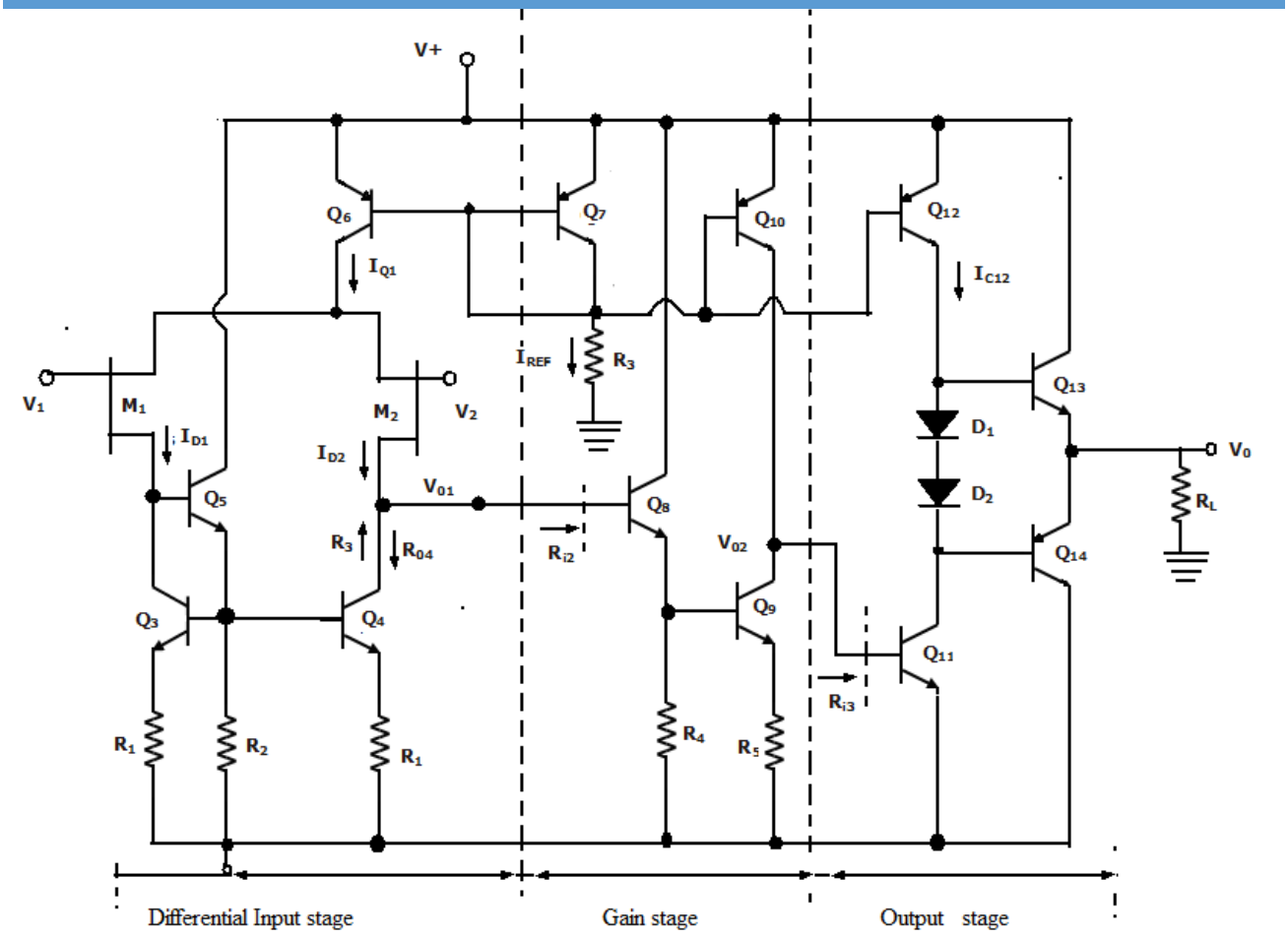
UNIT II

CHARACTERISTICS OF OPAMP

General Operational Amplifier:

An operational amplifier generally consists of three stages, anmely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter- follower or source follower output stage to provide current gain and low output resistance.

A low- frequency or dc gain of approximately 10^4 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. The figure shows a general op-amp circuit using JFET input devices.



Input stage:

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3 , Q_4 , and Q_5 . the bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the output resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5 . A single ended output is taken out at the collector of Q_4 .

MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input

resistance.Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9 . The V_{BE} drop across Q_9 and drop across R_5 constitute the voltage drop across R_4 , and this voltage sets the current through Q_8 . It can be set to a small value, such that the base current of Q_8 also is very less.

Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and $Q_{12,}$ through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain A_V of the op-amp is the product of voltage gain of each stage as given by

$A_V = |A_d ||A_2||A_3|$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. the input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V, and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current I_{REF} for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor $R_{5.}$ The widlar current source formed by Q_{11} , Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of $Q_{10.}$

Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The reference bias current I_{REF} also provides mirrored and proportional current at the collector of the double – collector lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13A} providing bias current for output stage and Q_{13B} providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two V_{BE} drops of potential difference between the bases of Q_{14} and Q_{18} .

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain.

The transistors Q5, Q6 and Q7 alo ng with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q_6. the two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q_3 and Q_4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q_3 and Q_4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20} . Hence, they provide an effective loss output resistance and current gain.

The output of the gain stage is connected at the base of Q_{22} , which is connected as an emitter – follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q_{13A} which also drives Q_{18} and Q_{19}, that are used for

establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.

Ideal op-amp characteristics:

1. Infinite voltage gain A.
2. Infinite input resistance R_i, so that almost any signal source can drive it and there is noloading of the proceeding stage.
3. Zero output resistance R_o, so that the output can drive an infinite number of other devices.
4. Zero output voltage, when input voltage is zero.
5. Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with outattenuation.
6. Infinite common mode rejection ratio, so that the output common mode noise voltage iszero.
7. Infinite slew rate, so that output voltage changes occur simultaneously with input voltagechanges.