## 4.1 8255-Program Pheripheral Interface (Programmable Peripheral input-output port)

The parallel input-output port chip 8255 is also called as programmableperipheral input-output port. The Intel‟s 8255 are designed for use with Intel‟s 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lineswhich may be individually programmed in two groups of twelve lines each, orthree groups of eight lines.

The two groups of I/O pins are named as Group A and Group B. Each of thesetwo groups contains a subgroup of eight I/O lines called as 8-bit port and anothersubgroup of four lines or a 4-bit port. Thus Group A contains an 8-bit port Aalong with a 4-bit port C upper.

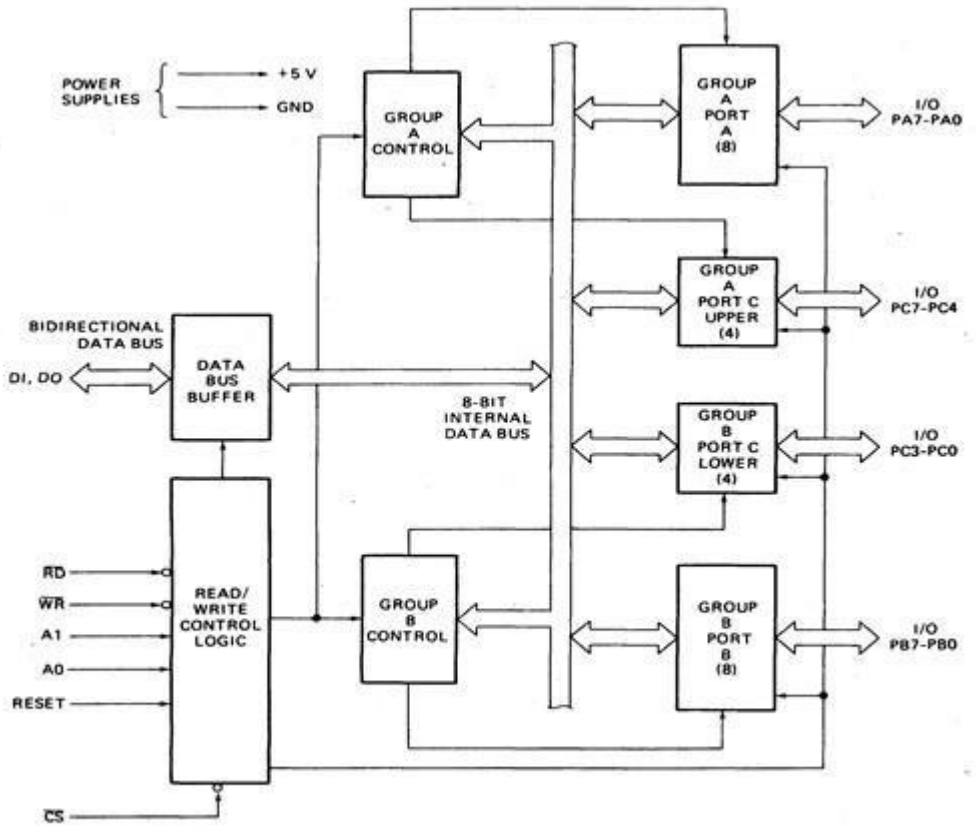


FIGURE Internal block diagram of 8255A programmable parallel port device. (*Intel Corporation*)

**Figure 4.1.1 Architecture**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*

The port A lines are identified by symbols PA0-PA7 while the port C lines are identified as PC4-PC7 similarly. Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0-PC3. The port C upper and port C lower can be used in combination as an 8-bit port C. Both the port Cs is assigned the same address.

Thus one may have either three 8-bit I/O ports or two 8-bit and two 4-bit I/O ports from 8255. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR). The internal block diagram and the pin configuration of 8255 are shown in figure 4.1.1.

The 8-bit data bus buffer is controlled by the read/write control logic. The read/write control logic manages all of the internal and external transfer of both data and control words. RD, WR, A1, A0 and RESET are the inputs, provided by the microprocessor to READ/WRITE control logic of 8255. The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus. This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

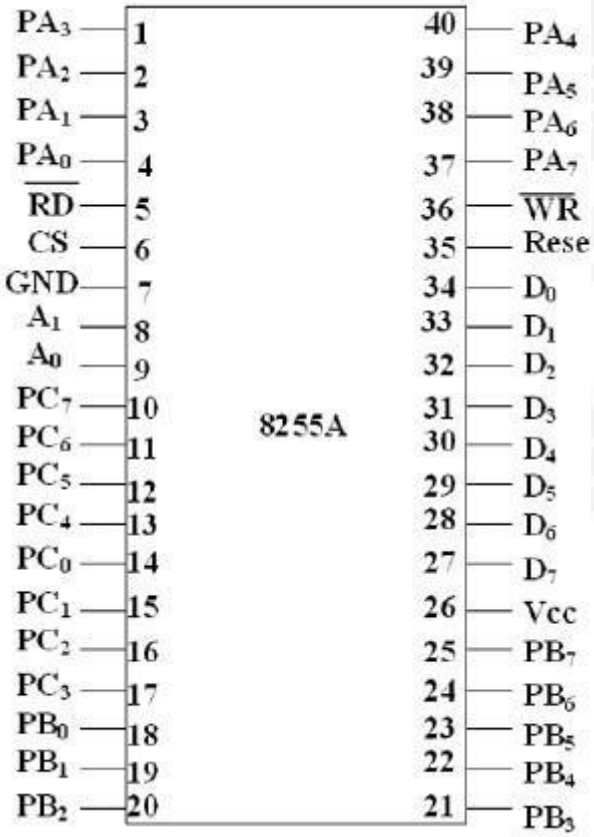


**Figure 4.1.2 Pin Diagram of 8255A**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*

- The port A lines are identified by symbols PA0-PA7 while the port C lines areIdentified as PC4-PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0- PC3. The port C upper and port C lower can be used in combination as an 8-bit port C.
- Both the port C is assigned the same address. Thus one may have either three 8-bit I/O ports or two 8-bit and two 4-bit ports from 8255. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR).
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- This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.
- PA7-PA0: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.
- PC7-PC4: Upper nibble of port C lines. They may act as either output latches or input buffers lines.
- This port also can be used for generation of handshake lines in mode1 or mode2.
- PC3-PC0: These are the lower port C lines; other details are the same as PC7- PC4 lines.
- PB0-PB7: These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.
- RD: This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.

- WR: This is an input line driven by the microprocessor. A low on this line indicates write operation.
- CS: This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.
- D0-D7: These are the data bus lines those carry data or control word to/from the microprocessor.
- RESET: Logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.
- A1-A0: These are the address input lines and are driven by the microprocessor.
- These lines A1-A0 with RD, WR and CS from the following operations for 8255. These address lines are used for addressing any one of the four registers, i.e. three ports and a control word register as given in table below.

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Input (Read) cycle |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | Port A to Data bus |
| 0 | 1 | 0 | 0 | 1 | Port B to Data bus |
| 0 | 1 | 0 | 1 | 0 | Port C to Data bus |
| 0 | 1 | 0 | 1 | 1 | CWR to Data bus |

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Output (Write) cycle |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | Data bus to Port A |
| 1 | 0 | 0 | 0 | 1 | Data bus to Port B |
| 1 | 0 | 0 | 1 | 0 | Data bus to Port C |
| 1 | 0 | 0 | 1 | 1 | Data bus to CWR |

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Function |
|---|---|---|---|---|---|
| X | X | 1 | X | X | Data bus tristated |
| 1 | 1 | 0 | X | X | Data bus tristated |

Control Word Register

**Figure 4.1.3 Control word Register of 8255A**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*

**Modes of Operation:**

- These are two basic modes of operation of 8255. I/O mode and Bit Set-Reset mode (BSR).
- In I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.

- Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications, mode 0, mode 1 and mode 2.
- BSR Mode: In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags D3, D2 and D1 of the CWR as given in table.

**I/O Modes:**

**1. Mode 0 (Basic I/O mode):**

This mode is also called as basic input/output Mode. This mode provides simple input and output capabilities using each of the threeports. Data can be simply read from and written to the input and output portsrespectively, after appropriate initialization.

| $D_3$ | $D_2$ | $D_1$ | Selected bits of port C |
|---|---|---|---|
| 0 | 0 | 0 | $D_0$ |
| 0 | 0 | 1 | $D_1$ |
| 0 | 1 | 0 | $D_2$ |
| 0 | 1 | 1 | $D_3$ |
| 1 | 0 | 0 | $D_4$ |
| 1 | 0 | 1 | $D_5$ |
| 1 | 1 | 0 | $D_6$ |
| 1 | 1 | 1 | $D_7$ |

BSR Mode : CWR Format

**Figure 4.1.4 Control word register of 8255A**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*

- Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combined used as a third 8-bit port.
- Any port can be used as an input or output port.
- Output ports are latched. Input ports are not latched.
- A maximum of four ports are available so that overall 16 I/O configurations are possible.
- All these modes can be selected by programming a register internal to 8255known as CWR.

- The control word register has two formats. The first format is valid for I/O modes of operation, i.e. modes 0, mode 1 and mode 2 while the second format is valid for bit set/reset (BSR) mode of operation.

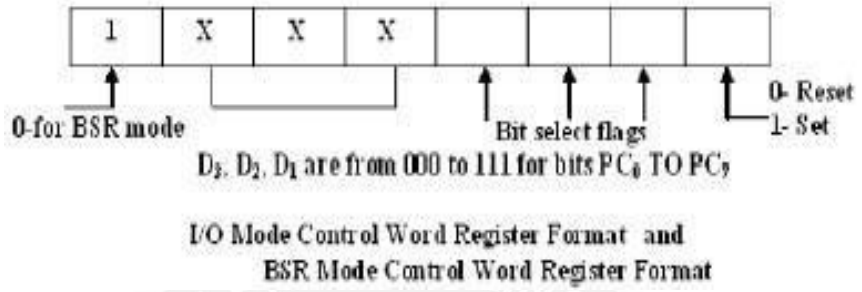


**Figure 4.1.5 Control word of 8255A**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*

2. **Mode 1: (Strobed input/output mode)**

In this mode the handshaking control the input and output action of the specified port. Port C lines PC0-PC2, provide strobe or handshake lines for port B. This group which includes port B and PC0-PC2 is called as group B for Strobed data input/output. Port C lines PC3-PC5 provides strobe lines for port A.This group including port A and PC3-PC5 from group A. Thus port C is utilized for generating handshake signals.

- Two groups – group A and group B are available for strobed data transfer.
- Each group contains one 8-bit data I/O port and one 4-bit control/data port.
- The 8-bit data port can be either used as input and output port. The inputs and outputs both are latched.
- Out of 8-bit port C, PC0-PC2 are used to generate control signals for port B andPC3-PC5 are used to generate control signals for port A. the lines PC6, PC7 may be used as independent data lines.
- OBF (Output buffer full) – This status signal, whenever falls to low, indicates that CPU has written data to the specified output port. The OBF flip- flop will beset by a rising edge of WR signal and reset by a low going edge at the ACK input.
- ACK (Acknowledge input) – ACK signal acts as an acknowledgement to be given by an output device. ACK signal, whenever low, informs the CPU that the data

transferred by the CPU to the output device through the port is received by the output device.

- INTR (Interrupt request) – Thus an output signal that can be used to interrupt the CPU when an output device acknowledges the data received from the CPU.INTR
- is set when ACK, OBF and INTE are 1. It is reset by a Falling edge on WR input. The INTEA and INTEB flags are controlled by the bit set- reset mode ofPC6 and PC2 respectively.

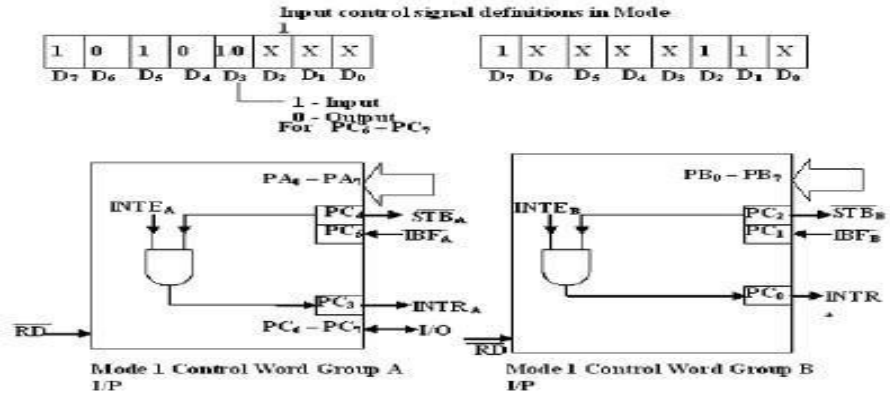


**Figure 4.1.6 Group A and Group B control of 8255A**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*

### 3.Mode 2 (Strobed bidirectional I/O):

This mode of operation of 8255 is also called as strobed bidirectional I/O. This mode of operation provides 8255 with additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. The interrupt generation and other functions are similar to mode1. In this mode, 8255 is a bidirectional 8-bit port with handshake signals. The Rd and WR signals decide whether the 8255 is going to operate as an input port or output port.

- The single 8-bit port in group A is available.
- The 8-bit port is bidirectional and additionally a 5-bit control port is available.
- Three I/O lines are available at port C.( PC2 – PC0 )
- Inputs and outputs are both latched.
- The 5-bit control port C (PC3-PC7) is used for generating/ accepting handshake signals for the 8-bit data transfer on port A.

- INTR – (Interrupt request) As in mode 1, this control signal is active high and is used to interrupt the microprocessor to ask for transfer of the next data byte to/from it. This signal is used for input (read) as well as output (write) operations.

Control Signals for Output operations:

- OBF (Output buffer full) – This signal, when falls to low level, indicates that the CPU has written data to port A.
- ACK (Acknowledge) This control input, when falls to logic low level, acknowledges that the previous data byte is received by the destination and next byte may be sent by the processor. This signal enables the internal tristate buffers to send the next data byte on port A.
- INTE1 ( A flag associated with OBF ) This can be controlled by bit set/reset mode with PC6.
- STB (Strobe input)a low on this line is used to strobe in the data into the input Latches of 8255.
- IBF (Input buffer full) when the data is loaded into input buffer, this signal rises to logic „1". This can be used as an acknowledge that the data has been received by the receiver.
- The waveforms in fig show the operation in Mode 2 for output as well as input port. Note: WR must occur before ACK and STB must be activated before RD.
- The following fig shows a schematic diagram containing an 8-bit bidirectional port, 5-bit control port and the relation of INTR with the control pins. Port B can either be set to Mode 0 or 1 with port A( Group A ) is in Mode 2.
- Mode 2 is not available for port B. The following fig shows the control word.
- The INTR goes high only if IBF, INTE2, STB and RD go high or OBF, INTE1, ACK and WR go high. The port C can be read to know the status of the peripheral device, in terms of the control signals, using the normal I/O instructions

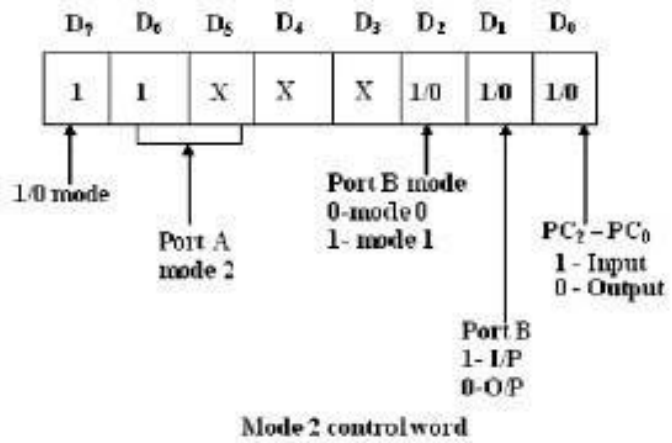


**Figure 4.1.7 Control word**

*[Source: "Microprocessor Architecture Programming and Application" by R.S. Gaonkar, page- ]*