2.3 Field Effect Transistor:

The field effect transistor is a semiconductor device, which depends for its operation on thecontrol of current by an electric field. There are two of field effect transistors:

- JFET (Junction Field Effect Transistor)
- MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Several advantages over conventional transistor.

- In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor. In FET the operation depends upon the flow of majority carriers only. It is called unipolar device.
- The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hencethe high input impedance of the order of M-ohm.
- It is less noisy than a bipolar transistor.
- It exhibits no offset voltage at zero drain current.
- It has thermal stability.
- It is relatively immune to radiation

The main disadvantage is its relatively small gain bandwidth product in comparison withconventional transistor.

Operation of FET:

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in fig. 2.3.1.

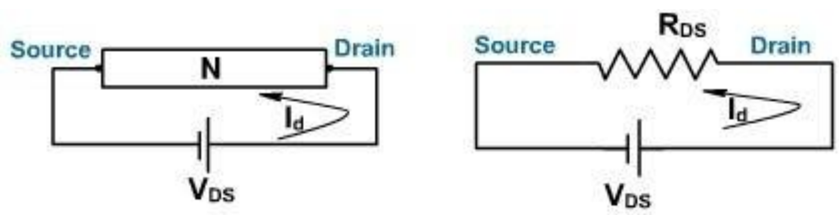


Figure: 2.3.1 FET in N-type semiconductor

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 210]

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel.

The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leaves the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS}. The resulting current is the drain current I_D. If V_{DS} increases, I_D Increases proportionally.

Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formedby any method for creating p n junction. These impurity regions are called gates (gate1 and gate2) as shown in fig. 2.3.2

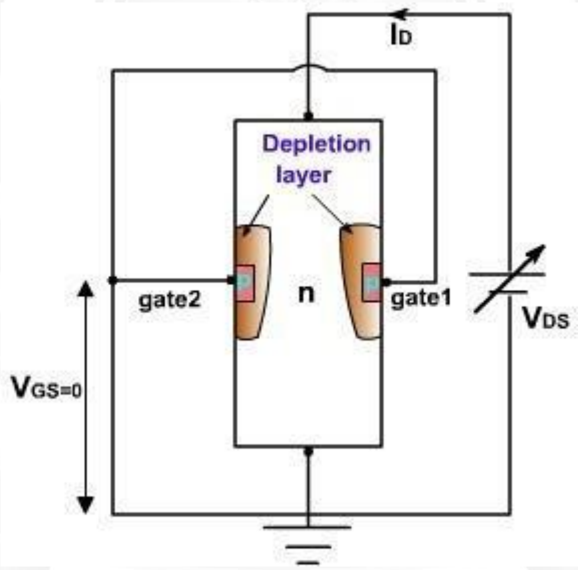


Figure: 2.3.2 N-channel device

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 210]

Both the gates are internally connected and they are grounded yielding zero gate source voltage (V_{GS} =0). The word gate is used because the potential applied between gate and source controlsthe channel width and hence the current.

As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The conductivity of this channel is normally zero because of the unavailability of current carriers.

The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, then points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the no conducting depletionregions. The width of this channel determines the resistance between drain and source.
Consider now the behavior of drain current I_D vs drain source voltage V_{DS}. The gate source voltage is zero therefore $V_{GS}= 0$. Suppose that V_{DS} is gradually linearly increased linearly from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The regionis called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch of voltage V_P**.

At this point further increase in V_{DS} do not produce corresponding increase in I_D. Instead, as V_{DS} increases, both depletion regions extend further into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is Called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS}. (Drain to source current with gate shorted)

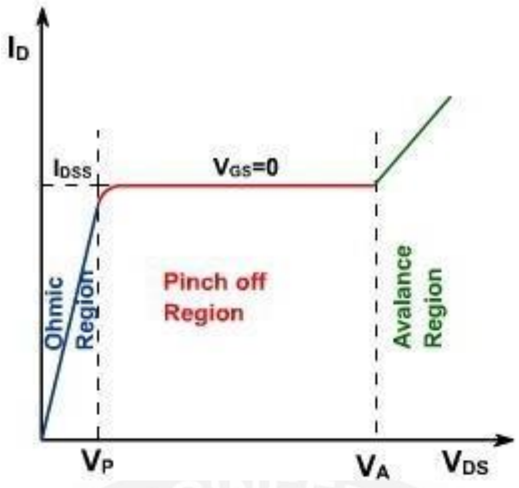
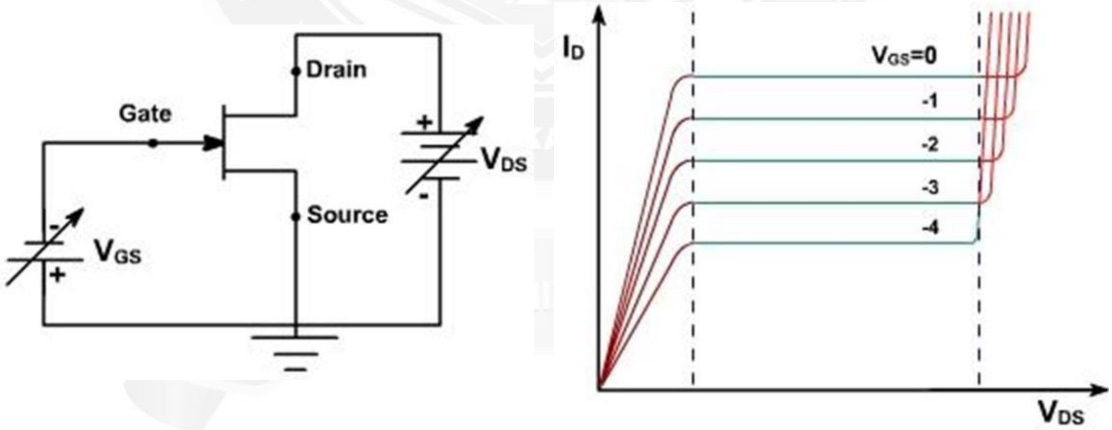


Figure: 2.3.3 P N junction occurs and ID rises

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 211]

As with all p n junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of p n junction occurs and I_D rises very rapidly as shown in fig. 2.3.3.

Consider now an N-channel JFET with a reverse gate source voltage as shown in **fig. 2.3.4.**



.

Figure: 2.3.4 JFET with a reverse gate source voltage

[Source: "Electronic devices and circuits" by "Balbir Kumar, Shail.B.Jain, and Page: 211]

The additional reverse bias, pinch off will occur for smaller values of | V_{DS} |, and the maximum drain current will be smaller. A family of curves for different values of V_{GS} (negative) is shown in **fig. 2.3.5**. Suppose that VGS= 0 and that due of VDS at a specific point along the channel is +5V with respect to ground.

Therefore reverse voltage across either p-n junction is now 5V. If VGS is decreased from 0 to –1V the net reverse bias near the point is 5 - (-1) = 6V. Thus for any fixed value of VDS, the channel width decreases as VGS is made more negative. Thus ID value changes correspondingly. When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized VGS (off). It is same as pinch off voltage.

Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the drain i.e. ID = IS. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.