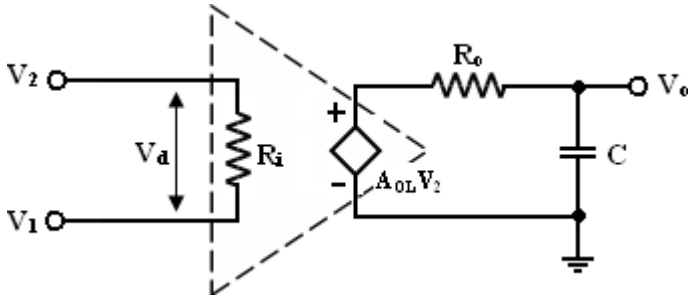
AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.

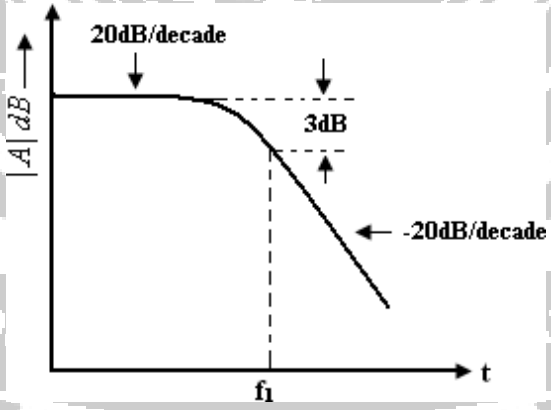


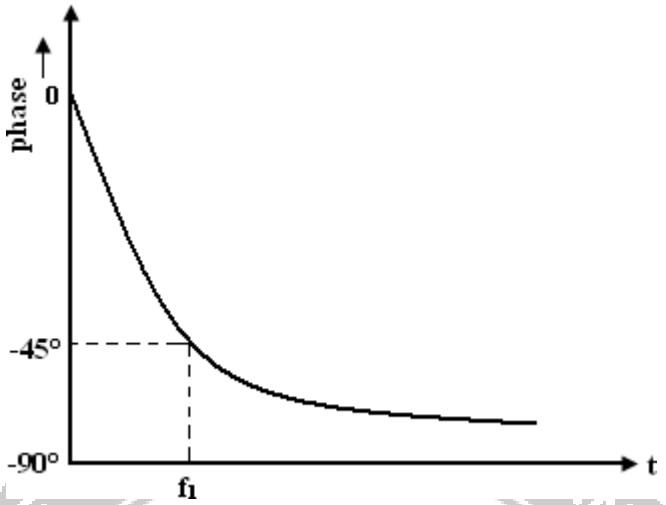
There is one pole due to R_0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig.

f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as,

The magnitude and phase angle characteristics from eqn (29) and (30)

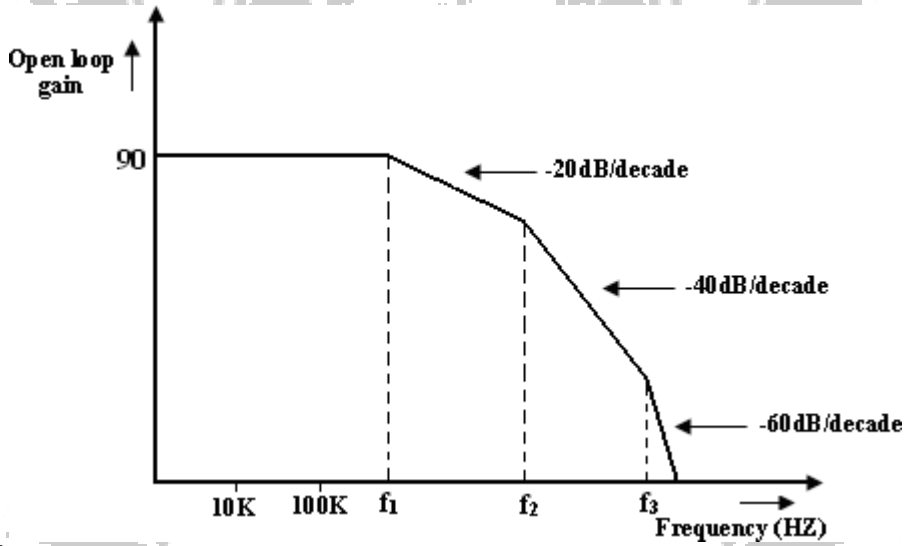
1. For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in dB.
2. At frequency f = f_1 the gain in 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.
3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or-6dB/decade.





From the phase characteristics that the phase angle is zero at frequency f =0.

At the corner frequency f_1 the phase angle is -45^0 (lagging and a infinite frequency the phase angle is -90^0 . It shows that a maximum of 90^0 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency.

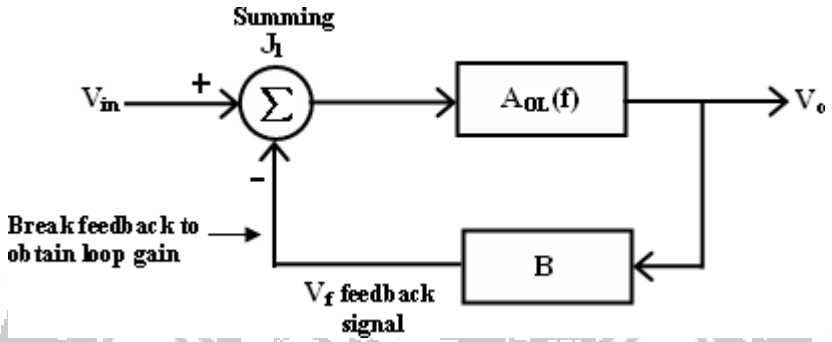


Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on inc reasing until the system break down. The unstable system are impractical and need be made stable. The

criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.



The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred –Transfer frequency' From fig we represented it by A_{OL} (f) which is given by

A_{OL} (f) = V_0 /Vin if V_f = 0------ (1)

where A_{OL} (f) = open loop volt gain. The closed loop gain A_f is given by

$A_F = V_0$ /Vin

$A_F = A_{OL}$ / (1+(A_{OL}) (B) ----- (2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method:1:

Determine the phase angle when the magnitude of (A_{OL}) (B) is 0dB (or) 1. If phase angle is > .-180^0 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (A_{OL}) (B) is 0dB (or) 1. If phase angle is > .-180^0 , If the magnitude is –ve decibels then the system is stable. However, the some systems the

phase angle of a system may reach -180^0 , under such conditions method 1 must be used to determine the system stability.

Slew Rate:

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{ ---------- (1)}$$

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

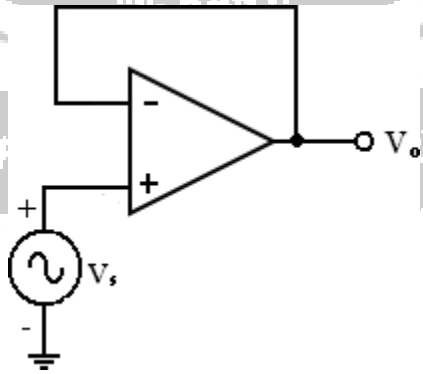
For 741 IC, the maximum internal capacitor charging current is limited to about 15μ A. So the slew rate of 741 IC is

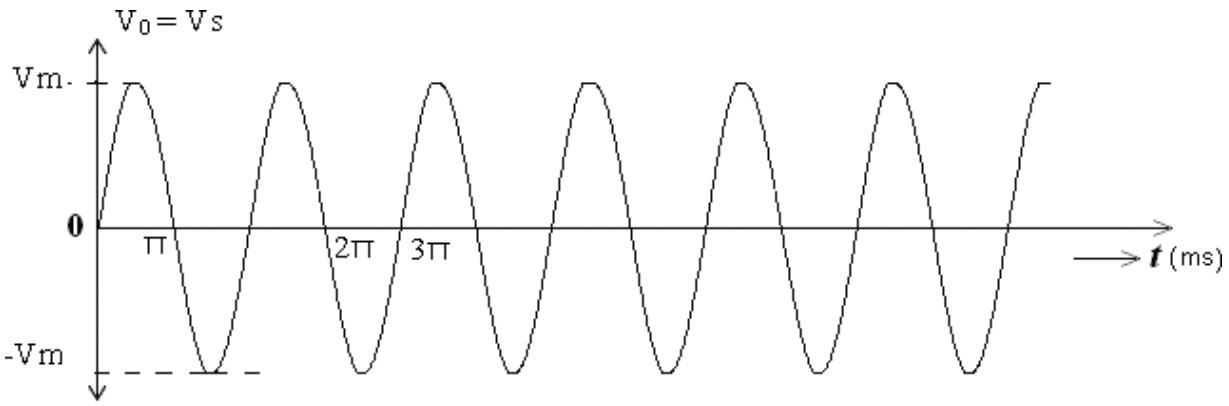
$$SR = dVc/dt\ |max = Imax/C .$$

For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .

If Vs = Vm Sinwt then output V_0 = Vm sinwt . The rate of change of output is given by

$$dV_0/dt = Vm\ w\ coswt.$$





Input and Output Waveforms

The max rate of change of output across when coswt =1

(i.e) SR = $dV_0/dt|max = wVm$.

SR = 2∏fVm V/s = 2∏fVm v/ms.

Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by

fmax (Hz) = Slew rate/6.28 * Vm .

called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

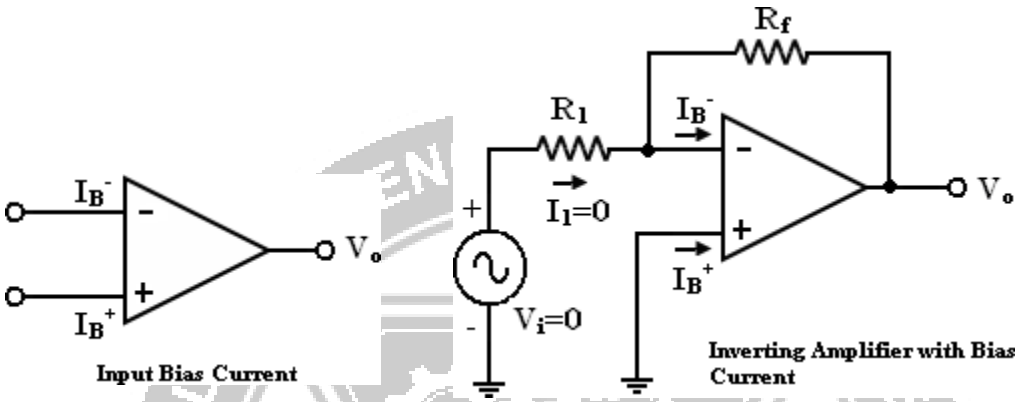
1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

Input bias current:

The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

- In an ideal op-amp, we assumed that no current is drawn from the input terminals.
- The base currents entering into the inverting and non-inverting terminals

- Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs.
- Manufacturers specify the input bias current I_B



So, $I_B = \frac{I_B^- + I_B^+}{2}$ (1)

If input voltage $V_i = 0V$. The output Voltage V_o should also be ($V_o = 0$)

$I_B = 500nA$

We find that the output voltage is offset by,

$$V_o = I_B R_f \quad (2)$$

Op-amp with a 1M feedback resistor

$V_o = 5000nA \times 1M = 500mV$

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated. Where a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$$-V_1+0+V_2-V_o = 0 \text{ (or)}$$

$$V_o = V_2 - V_1 \quad \text{——>(3)}$$

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived a

$$V_1 = I_B^+ R_{comp} \text{ (or)}$$

$$I_B^+ = V_1 / R_{comp} \quad \text{——>(4)}$$

The node _a' is at voltage ($-V_1$). Because the voltage at the non-inverting input terminal is ($-V_1$). So with $V_i = 0$ we get,

$$I_1 = V_1/R_1 \quad \text{——>(5)}$$

$$I_2 = V_2/R_f \quad \text{——>(6)}$$

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$$I_2 = V_1/R_f \quad \text{——>(7)}$$

KCL at node _a' gives,

$$I_B^- = I_2 + I_1$$

$$I_B = \frac{R_f}{R_1}$$

Assume $I_B^- = I_B^+$ and using equation (4) & (8) we get

$$R_{comp} = R_1 \parallel R_f$$

$$R_{comp} = R_1 \parallel R_f \quad \text{———>(9)}$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

- Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.
- Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$|I_{os}| = I_B^+ - I_B^-$ ——>(10)

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$V_1 = I_B^+ R_{comp}$ ——>(11)

And $I_1 = V_1/R_1$ ——>(12)

KCL at node ‗a' gives,

Again

$V_0 = I_2 R_f - V_1$

$V_o = I_2 R_f - I_B^+ R_{comp}$

$V_o = 1M\ \Omega \text{ X } 200nA$

$V_o = 200mV$ with $V_i = 0$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R_1 must be kept large.
- R_1 large, the feedback resistor R_f must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

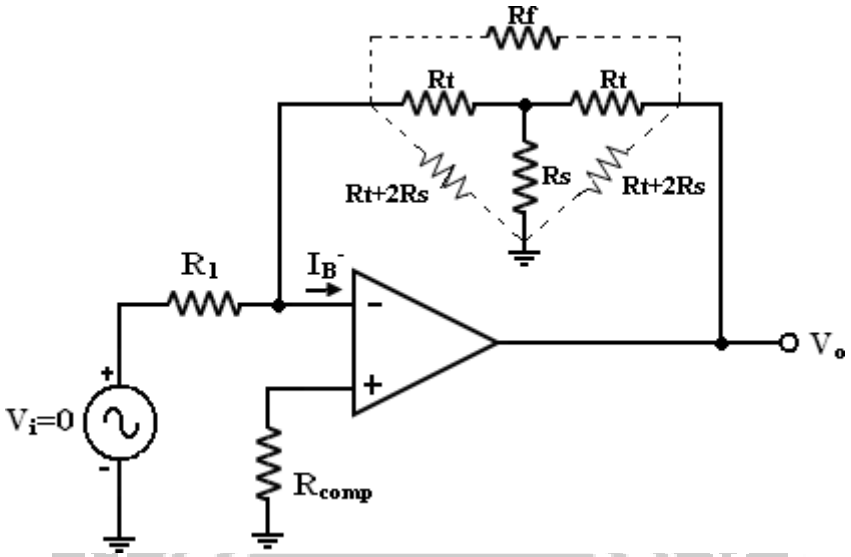
- The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

To design T- network first pick $R_t << R_f/2$ ——>(18)

Then calculate R_s [

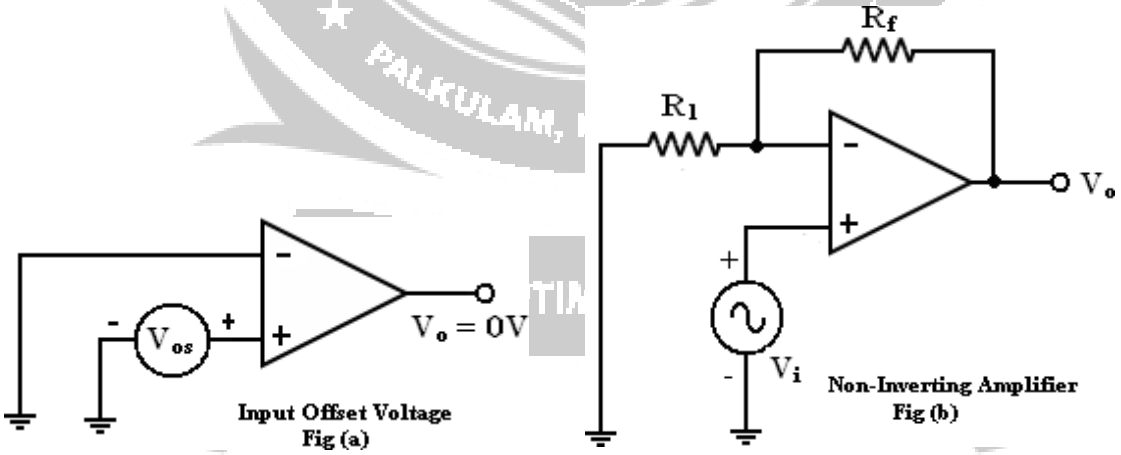
$R_f \quad 2R_t$

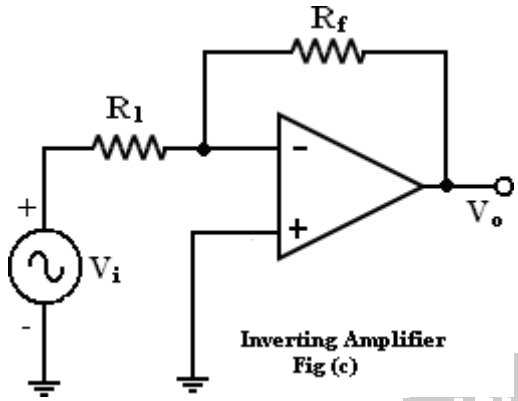


Input offset voltage:

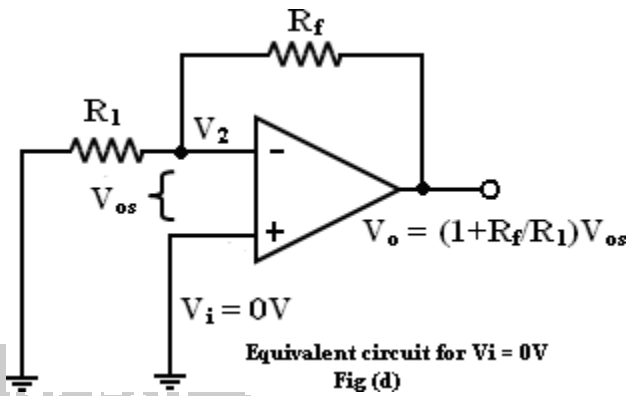
Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [$V_o \neq 0$ with $V_i = 0$]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (V_o) = 0.

This voltage is called input offset voltage V_{os}. This is the voltage required to be applied at the input for making output voltage to zero ($V_o = 0$).





Inverting Amplifier
Fig (c)



Equivalent circuit for Vi = 0V
Fig (d)

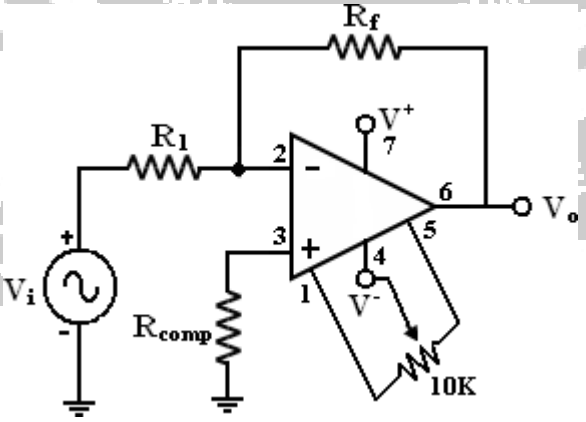
Let us determine the V_{os} on the output of inverting and non- inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

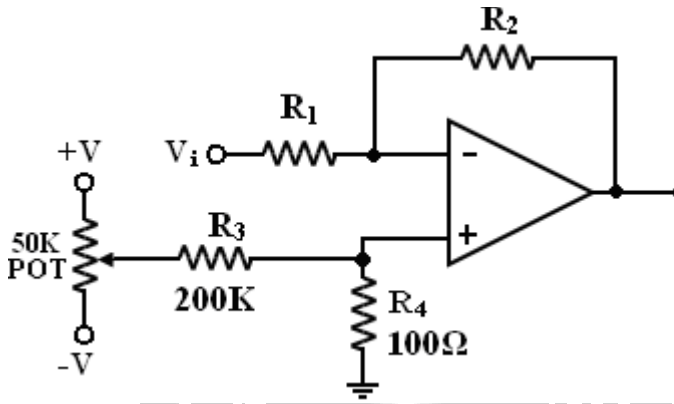
The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone(V_{os}).

This is because I_B and V_{os} could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non- inverting amplifier (figure b, c) without any compensation technique used is given by many op-amp provide offset compensation pins to nullify the offset voltage.

- 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4.
- The position of the wipes is adjusted to nullify the offset voltage.



When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.



$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$