3.6 INSTRUCTION SET

The microcontroller 8051 instructions set includes 110 instructions, 49 of which are single byte instructions, 45 are two bytes instructions and 17 are three bytes instructions. The instructions format consists of a function mnemonic followed by destination and source field.

ADDRESSING MODES OF 8051 :

The way in which the data operands are accessed by different instructions is known as the addressing modes. There are various methods of denoting the data operands in the instruction. The 8051 microcontroller supports mainly 5 addressing modes. They are

1.Immediate addressing mode

2.Direct Addressing mode

3.Register addressing mode

4. Register Indirect addressing mode

5.Indexed addressing mode

Immediate addressing mode :

The addressing mode in which the data operand is a constant and it is a part of the instruction itself is known as Immediate addressing mode. Normally the data must be preceded by a # sign. This addressing mode can be used to transfer the data into any of the registers including DPTR.

Ex: MOV A , # 27 H : The data (constant) 27 is moved to the accumulator register

ADD R1 ,#45 H : Add the constant 45 to the contents of the accumulator

MOV DPTR ,# 8245H :Move the data 8245 into the data pointer register.

MOV P1,#21 H

Direct addressing mode:

The addressing mode in which the data operand is in the RAM location (00 -7FH) and the address of the data operand is given in the instruction is known as Direct addressing mode. The direct addressing mode uses the lower 128 bytes of Internal RAM and the SFRs

MOV R1, 42H : Move the contents of RAM location 42 into R1 register

MOV 49H,A : Move the contents of the accumulator into the RAM location 49.

ADD A, 56H : Add the contents of the RAM location 56 to the accumulator

Register addressing mode :

The addressing mode in which the data operand to be manipulated lies in one of the registers is known as register addressing mode.

MOV A,R0 : Move the contents of the register R0 to the accumulator

ADD A,R6 :Add the contents of R6 register to the accumulator

MOV P1, R2 : Move the contents of the R2 register into port 1

MOVR5, R2: This is invalid .The data transfer between the registers is not allowed.

Register Indirect addressing mode :

The addressing mode in which a register is used as a pointer to the data memory block is known as Register indirect addressing mode.

MOV A,@ R0 :Move the contents of RAM location whose address is in R0 into A (accumulator)

MOV @ R1 , B : Move the contents of B into RAM location whose address is held by R1

When R0 and R1 are used as pointers, they must be preceded by @ sign,One of the advantages of register indirect addressing mode is that it makes accessing the data more dynamic than static as in the case of direct addressing mode.

Indexed addressing mode :

This addressing mode is used in accessing the data elements of lookup table entries located in program ROM space of 8051.

Ex : MOVC A,@ A+DPTR

The 16-bit register DPTR and register A are used to form the address of the data element stored in on-chip ROM. Here C denotes code .In this instruction the contents of A are added to the 16-bit DPTR register to form the 16-bit address of the data operand.

INSTRUCTION SET OF 8051 MICROCONTROLLER

All members of the 8051 family execute the same instructions set. The 8051 instructions set is optimized for 8-bit content application. The Intel 8051 has excellent and most powerful instructions set offers possibilities in control area, serial Input/Output, arithmetic, byte and bit manipulation.

It has 111 instructions they are

- 49 single byte instructions

- 45 two bytes instructions
- 17 three bytes instructions

The- instructions set is divided into four groups, they are

- Data transfer instructions
- Arithmetic instructions
- Logical instructions
- Call and Jump instructions

DATA TRANSFER INSTRUCTIONS

This instruction copies the contents of the source location to the destination location. The contents of the source location are unchanged.

Instruction format	Algorithm	Example	Functon
MOVA, Rn	A = Rn	MOV A, R1	Move byte form register Rn to accumulator
MOV A, direct	A = direct	MOV A, 40H	Move byte from direct address to accumulator
MOV A, @ Ri	A=[[Ri]]	MOVA,@ R0	Move the content of memory location to accumulator
MOV A, # data	A = # data	MOV A, #31 H	Move immediate data to accumulator
MOV Rn, A	Rn = A	MOV R5, A	Move data from accumulator to register Rn
MOV Rn, direct	Rn = direct	MOV R3, 30H	Move data from direct address to register Rn.
MOV Rn, # data	Rn = # data	MOV R7, #20H	Move immediate data to register Rn.
MOV direct, A	direct =A	MOV 80H, A	Move data from accumulator to direct address
MOV direct, Rn	direct = Rn	MOV 30H, R5	Move data from register to direct address

MOV direct, direct	direct = direct	MOV 20H, 30H	Move data form source direct address to the destination direct address.
MOV direct, @Ri	direct = [[Ri]]	MOV 20H, @R1	Move data from address specified in register Ri to direct address.
MOV direct, #data	direct = #data	MOV 10H, #10H	Move immediate data to direct address
MOV @Ri, A	[[Ri]] = A	MOV @ R0,A	Move data form accumulator to memory location pointed by Ri

ARITHMETIC INSTRUCTIONS:

Mnemonic	Example	Description
ADD A, Rn	ADD A, R0	This instruction will add the byte in register Rn of the selected register bank with the byte in accumulator. The result is contained in the accumulator
ADD A, direct	ADD A, 20H	This instruction will add the contents of the memory location whose direct address is specified in the instruction with the accumulator contents. The result of addition will he stored in the accumulator.
ADD A, @ Ri	ADD A, @ R0	This instruction will add the contents of memory location whose address is pointed by register Ri of the selected register bank with contents of the accumulator. The result of addition is stored in the accumulator
ADD A, # data	ADD A, # 30H	This instruction will add the immediate 8 bit data with data in the accumulator. The result of addition is stored in the accumulator.

Mnemonics	**Addressing mode**	**Example**	**Description**
ADDC A, Rn	Register addressing	ADDC A, Rl	This instruction will add the contents of accumulator with the contents of register Rn of the selected register bank and carry flag. The result of addition is stored in accumulator.
ADDC A, direct	Direct addressing	ADDC A, 10H	This instruction will add the contents of memory location whose direct address is specified in the instruction with the contents of accumulator and carry. The result of addition is stored in the accumulator.
ADDC A, @Ri	Register Indirect	ADDC A, @R0	This instruction will add the contents of memory location pointed by register Ri of selected register bank with the accumulator and earn' flag. The result is stored in accumulator.
ADDC A, #data	Immediate addressing	ADDC A, #40H	This instruction will add the contents of accumulator with immediate data specified in the instruction along with carry.
ADDC A, Rn	Register addressing	ADDC A, Rl	This instruction will add the contents of accumulator with the contents of register Rn of the selected register bank and carry flag. The result of addition is stored in accumulator.

ADDC A, direct	Direct addressing	ADDC A, 10H	This instruction will add the contents of memory location whose direct address is specified in the instruction with the contents of accumulator and carry. The result of addition is stored in the accumulator.
ADDC A, @Ri	Register Indirect	ADDC A, @R0	This instruction will add the contents of memory location pointed by register Ri of selected register bank with the accumulator and earn' flag. The result is stored in accumulator.
ADDC A, #data	Immediate addressing	ADDC A, #40H	This instruction will add the contents of accumulator with immediate data specified in the instruction along with carry.

LOGICAL INSTRUCTIONS:

Mnemonics	Addressing mode	Example	Description
ANL A, Rn	Register addressing	ANL A, R5	This instruction will perform bit wise logical AND operation between the contents of accumulator and register Rn of the selected register bank. The result will be stored in the accumulator
ANL A, direct	Direct addressing	ANL A, 70H	This instruction will bit wise logically AND the contents of accumulator with the contents of memory location whose direct address is specified in the instruction. The result will be stored in the accumulator
ANL direct, A	Direct addressing	AXL 30H, A	This instruction will bit wise logically AND the contents of memory location whose direct address is specified in the instruction with the contents of accumulator. The result will be stored

			in the memory location whose direct address is specified in the instruction.
ANL A, ®Ri	Register Indirect Addressing	ANL A, @R1	This instruction will bit wise logically AND the contents of accumulator with the contents of memory location pointed by register Ri of the selected register bank. The result will be stored
ANL A, #data	Immediate addressing	ANL A, #57H	This instruction will bit wise logically AND the contents of accumulator with the immediate data specified in the instruction. The result will be stored in the accumulator.
ANL direct, #data	Immediate addressing	ANL 54H, #33H	This instruction will bit wise logically AND the contents of memory location whose direct address is specified in the instruction with the contents of with the immediate data specified in the instruction. The result will be stored in the memory location whose direct address is specified in the instruction.

CLRA

- This instruction will clear all the bits of accumulator to zero.

CPLA

- This instruction will complements all the bits (l's complement) of the accumulator.

RLA

- This instruction will rotate the eight bits in the accumulator by one bit to the left.
- Addressing mode: Register Specific addressing mode.

RLCA

- This instruction will rotate the eight bits in the accumulator and the carry flag together by one bit to the left
- Addressing mode: Register Specific addressing mode.

RRA

- This instruction will rotate the eight bits in the accumulator by one bit to the right.
- Addressing mode: Register Specific addressing mode.

RRCA

- This instruction will rotate the eight bits in the accumulator and the carry flag together by one bit to the right.
- Addressing mode: Register Specific addressing mode.

SWAP A

This instruction interchanges the low order and high order nibbles of the accumulator. Operation:

- Addressing mode: Register Specific addressing mode.