# HIGH SPEED SAMPLE AND HOLD CIRCUITS

**Introduction:**

Sample-and- hold (S/H) is an important analog building block with many applications, ncluding analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where Vin is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.Ch

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever

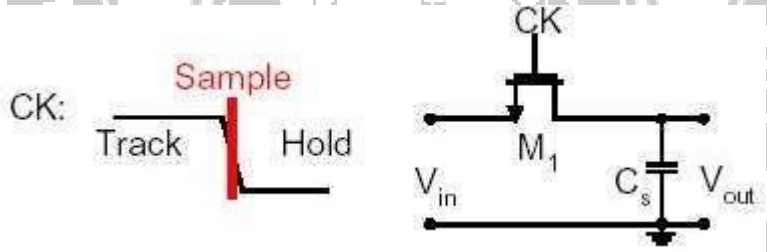



**Figure 1: Simplest sample-and-hold circuit in MOS technology.**

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever ck is high, the MOS switch is on, which in turn allows Vout to track Vin. On the other hand, when ck is low, the MOS switch is off. During this time, Ch will keep Vout equal to the value of Vin at the instance when ck goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as descr ibed

above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

**Alternative CMOS Sample-and-Hold Circuits:**

This section covers three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feedthrough.

Series Sampling:

The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled.

On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.

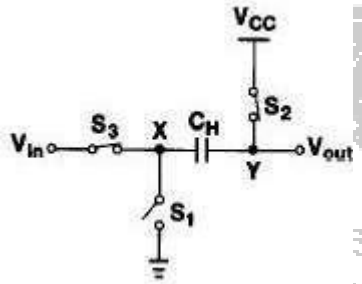



**Figure 2: Series sampling.**

When the circuit is in sample mode, both switches *S2* and *S3* are on, while *S1* is off. Then,*S2* is turned off first, which means *Vout* is equal to *VCC* (or *VDD* for most circuits) and the voltage drop across *Ch* will be *VCC – Vin*. Subsequently, *S3* is turned off and *S1* is turned on simultaneously. By grounding node *X*, *Vout* is now equal to *VCC – Vin*, and the drop from *VCC* to *VCC – Vin* is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because *S2* is turned off before *S3*. Thus, the fact that the gate-to-source voltage, *VGS*, of *S2* is constant means that charge injection coming from *S2* is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node *Y*. This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that *Ch* be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of *Vout* in series sampling is being reset to *VCC* (or *VDD*) for every sample, but this is not the casefor parallel sampling.

**Switched Op-Amp Based Sample-and-Hold Circuit:**

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure 3.

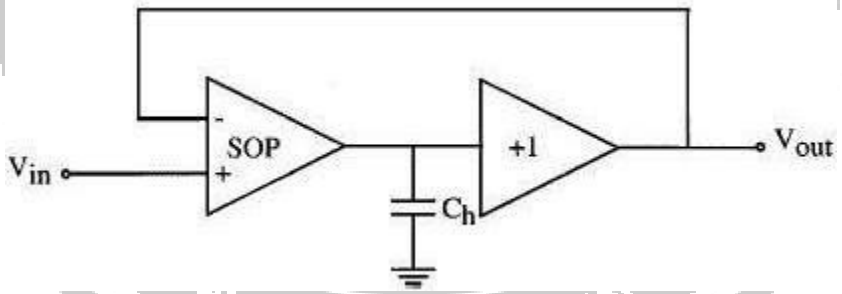



**Figure 3: Switched op-amp based sample and hold circuit.**

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on Ch to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on Ch to the output of the S/H circuit.

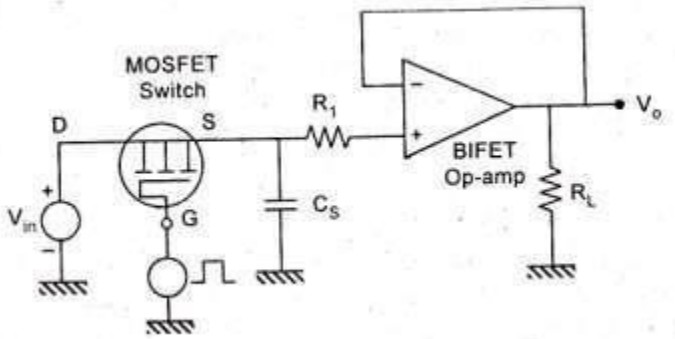
With the increasing demand for high-resolution and high-speed in date acquisition systems, the performance of the S/H circuits is becoming more and more important. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits

that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. As a result of this, new researches in analog

circuits are now shifted from voltage- mode to current-mode. The advantages of current mode circuits include low- voltage, low-power, and high-speed. Therefore, future

researches of S/H circuit should also shift toward current-mode S/H techniques.

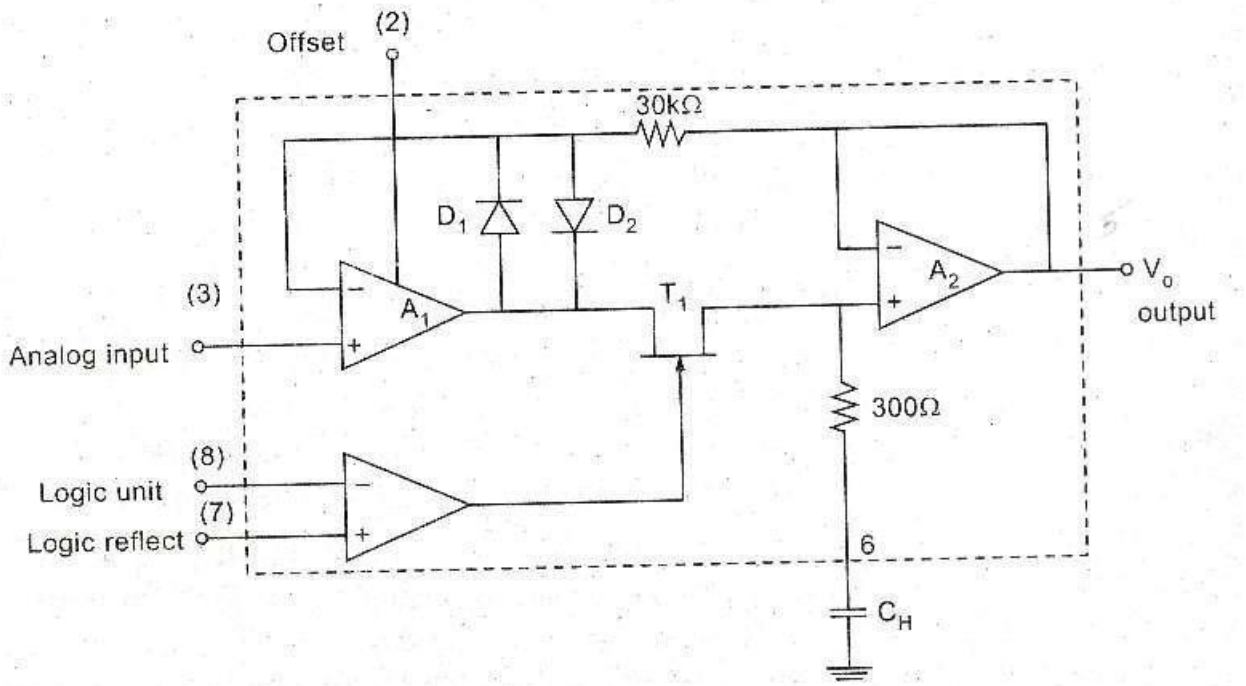



The above figure shows a sample and hold circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

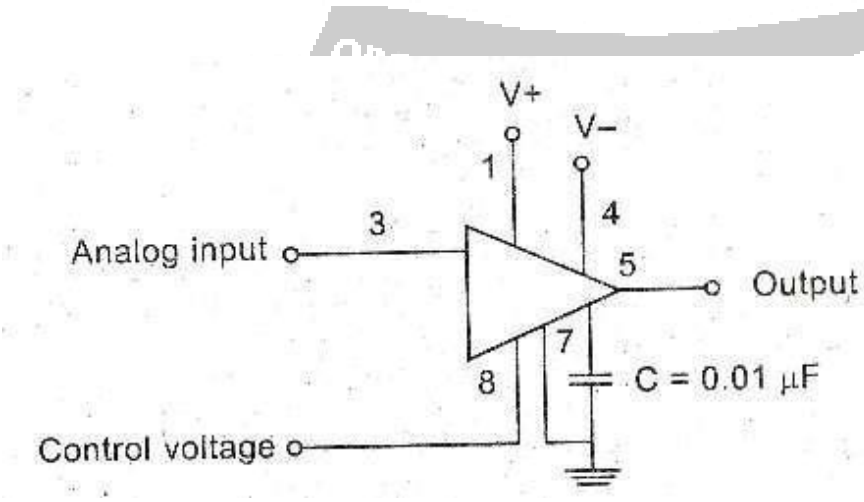
Sample-and- hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor.

However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feed through restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order to meet the increasing demand for high-speed, low-power, and low voltage S/H circuits for data acquisition systems.

**LF 398 IC- Functional Diagram**



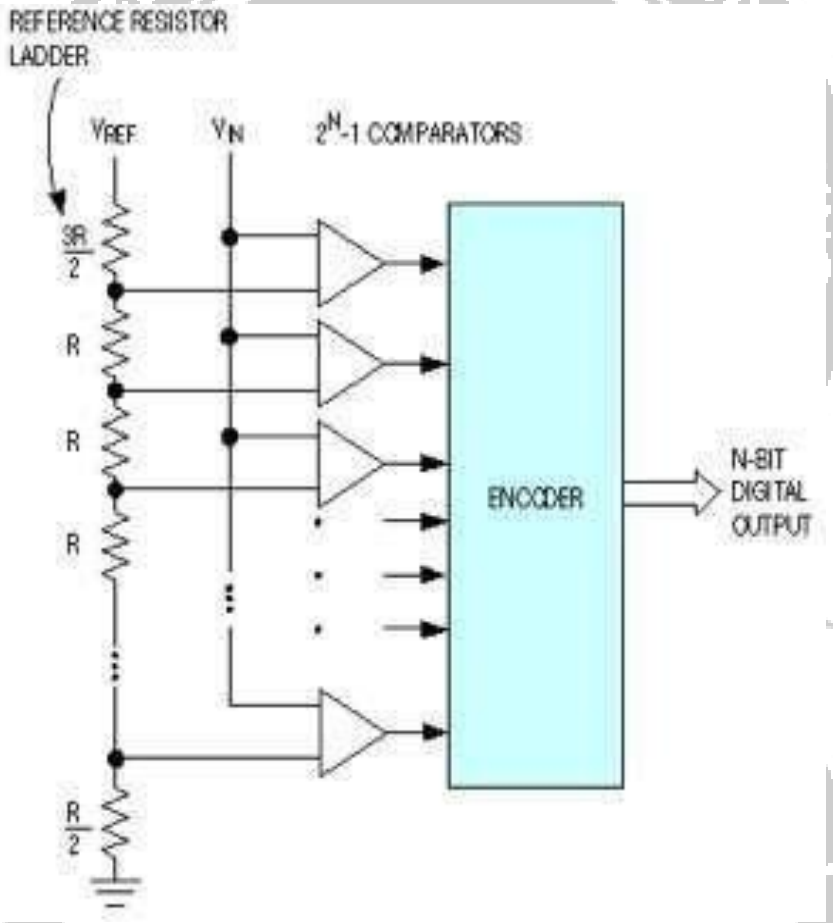

**Connection Diagram**



**Types of ADC**

**Direct-conversion ADC/Flash type ADC:**

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.

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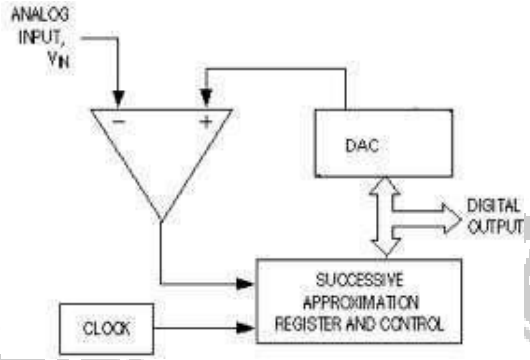
**Successive-approximationADCs**

Successive-approximation ADC is a conversion technique based on a successive-approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC). The final result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit ( MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz

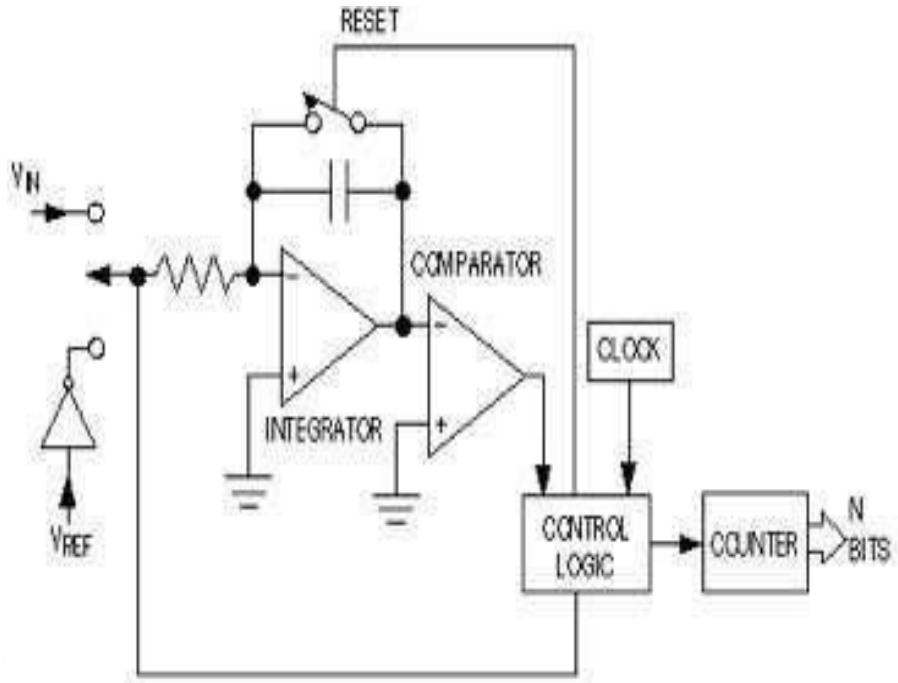
would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.




**IntegratingADCs**

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again. The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high- frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi- meters.

An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run- up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run- up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.




**Sigma-delta ADCs/ Over sampling Converters:**

It consist of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transform by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, low noise and low cost. Typical applications are for speech and audio.

A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)

**A/D Using Voltage to time conversion**:

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed- frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram, A negative reference voltage -VR is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va. At t = T, Vc goes low and switch S remains open. When VEN goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.