Transistor Fabrication:

PNP Transistor:

The integrated PNP transistors are fabricated in one of the following three structures.

1. Substrate or Vertical PNP
2. Lateral or horizontal PNP and
3. Triple diffused PNP

Substrate or Vertical PNP:

The P-substrate of the IC is used as the collector, the N-epitaxial layer is used as the base and the next P-diffusion is used as the emitter region of the PNP transistor. The structure of a vertical monolithic PNP transistor Q_1 is shown in figure. The base region of an NPN transistor structure is formed in parallel with the emitter region of the PNP transistor.

The method of fabrication has the disadvantage of having its collector held at a fixed negative potential. This is due to the fact that the P-substrate of the IC is always held at a negative potential normally for providing good isolation between the circuit components and the substrate.

Triple diffused PNP:

This type of PNP transistor is formed by including an additional diffusion process over the standard NPN transistor processing steps. This is called a triple diffusion process, because it involves an additional diffusion of P-region in the second N-diffusion region of a NPN transistor. The structure of the triple diffused monolithic PNP transistor Q_2 is also shown in the below figure.

This has the limitations of requiring additional fabrication steps and sophisticated fabrication assemblies.

Lateral or Horizontal PNP:

This is the most commonly used form of integrated PNP transistor fabrication method. This has the advantage that it can be fabricated simultaneously with the processing steps of an NPN transistor and therefore it requires as the base of the PNP transistor. During the P-type base diffusion process of NPN transistor, two parallel P-regions are formed which make the emitter and collector regions of the horizontal PNP transistor.

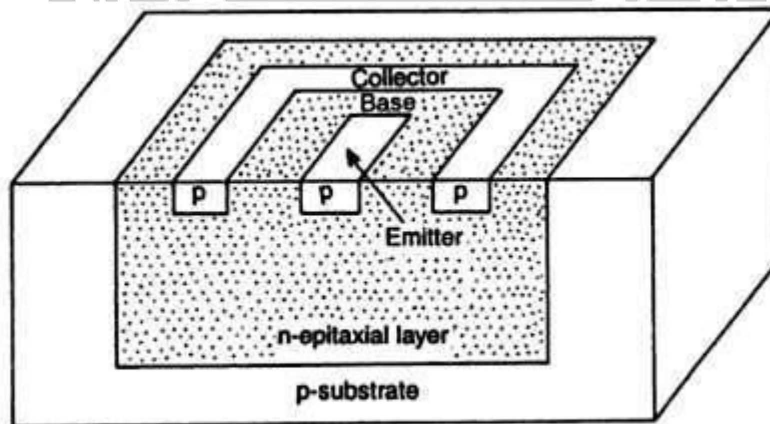


Fig. 1.17 A *pnp* lateral transistor

Comparison of monolithic NPN and PNP transistor:

Normally, the NPN transistor is preferred in monolithic circuits due to the following reasons:

1. The vertical PNP transistor must have his collector held at a fixed negative voltage.

2. The lateral PNP transistor has very wide base region and has the limitation due to the lateral diffusion of P-type impurities into the N-type base region. This makes the photographic mask making, alignment and etching processes very difficult. This reduces the current gain of lateral PNP transistors as low as 1.5 to 30 as against 50 to 300 for a monolithic NPN transistor.

3. The collector region is formed prior to the formation of base and emitter diffusion. During the later diffusion steps, the collector impurities diffuse on either side of the defined collector junction. Since the N-type impurities have smaller diffusion constant compared to P-type impurities the N-

type collector performs better than the P-type collector. This makes the NPN transistor preferable for monolithic fabrication due to the easier process control.

Transistor with multiple emitters: The applications such as transistor- transistor logic (TTL) require multiple emitters. The below figure shows the circuit sectional view of three N-emitter regions diffused in three places inside the P-type base. This arrangement saves the chip area and enhances the component density of the IC.

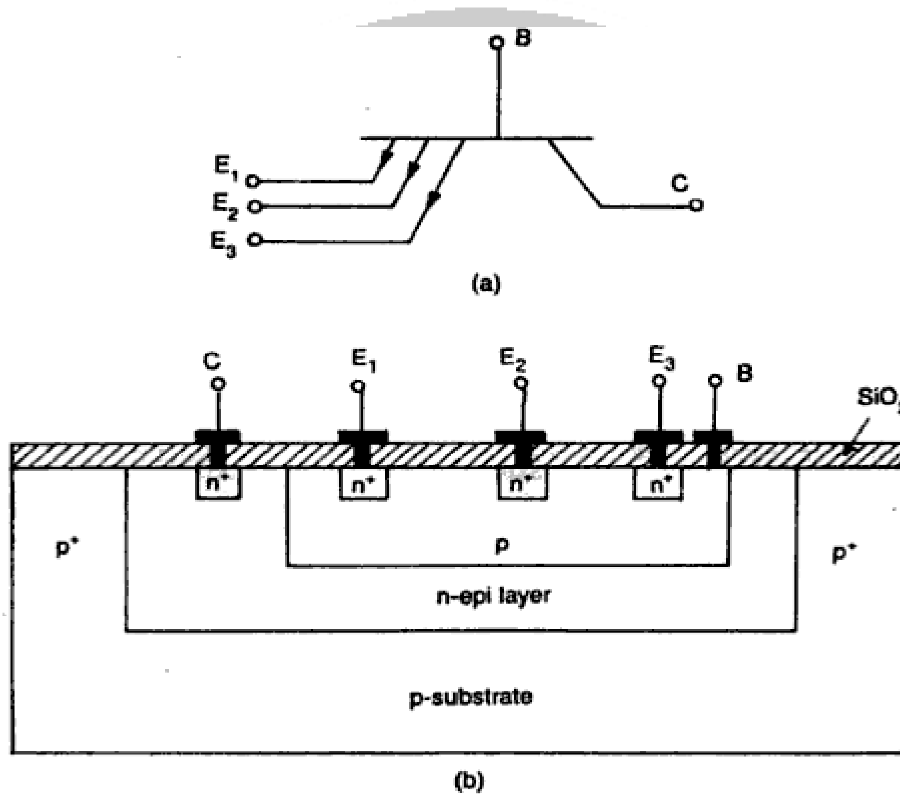


Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

Schottky Barrier Diode:

OBSERVE OPTIMIZE OUTSPREAD

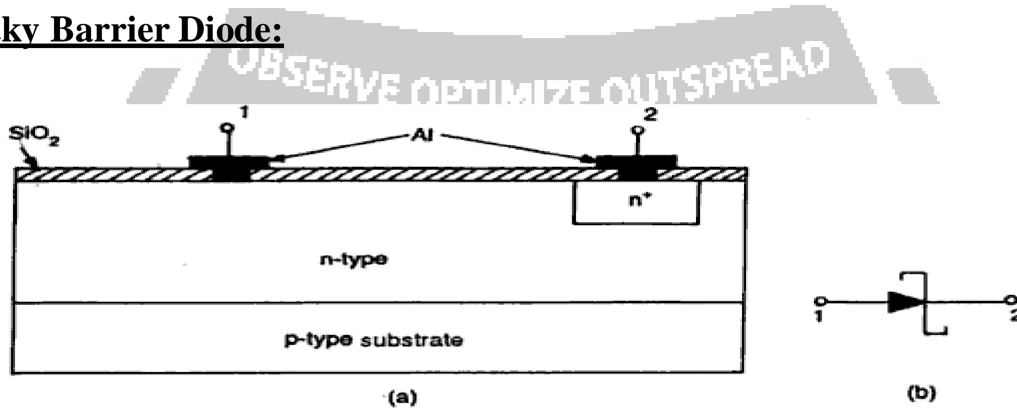


Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

The metal contacts are required to be ohmic and no PN junctions to be formed between the metal and silicon layers. The N^+ diffusion region serves the purpose of generating ohmic contacts. On the other hand, if aluminum is deposited directly on the N-type silicon, then a metal semiconductor diode can be said to be formed. Such a metal semiconductor diode junction exhibits the same type of V-I Characteristics as that of an ordinary PN junction.

The cross sectional view and symbol of a Schottky barrier diode as shown in figure. Contact 1 shown in figure is a Schottky barrier and the contact 2 is an ohmic contact. The contact potential between the semiconductor and the metal generated a barrier for the flow of conducting electrons from semiconductor to metal. When the junction is forward biased this barrier is lowered and the electron flow is allowed from semiconductor to metal, where the electrons are in large quantities.

The minority carriers carry the conduction current in the Schottky diode whereas in the PN junction diode, minority carriers carry the conduction current and it incurs an appreciable time delay from ON state to OFF state. This is due to the fact that the minority carriers stored in the junction have to be totally removed. This characteristic puts the Schottky barrier diode at an advantage since it exhibits negligible time to flow the electron from N-type silicon into aluminum almost right at the contact surface, where they mix with the free electrons. The other advantage of this diode is that it has less forward voltage (approximately 0.4V). Thus it can be used for clamping and detection in high frequency applications and microwave integrated circuits.

Schottky transistor:

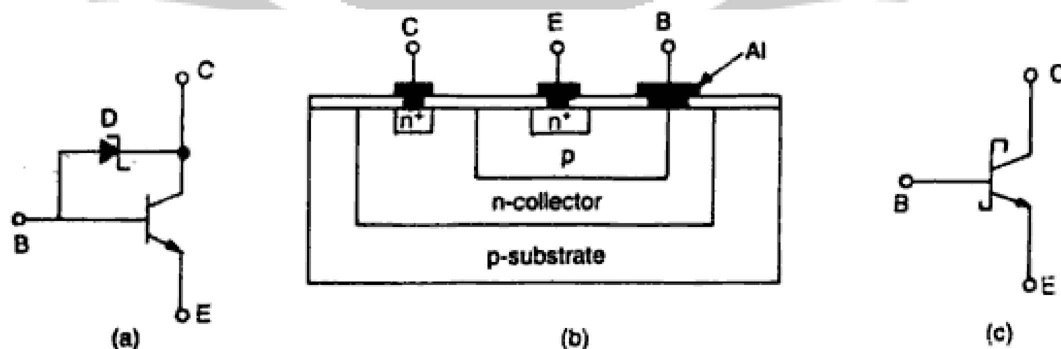


Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

The cross-sectional view of a transistor employing a Schottky barrier diode clamped between its base and collector regions is shown in figure. The equivalent circuit and the symbolic representation of the Schottky transistor are shown in figure. The Schottky diode is formed by allowing aluminium metallization for the base lead which makes contact with the N-type collector region also as shown in figure.

When the base current is increased to saturate the transistor, the voltage at the collector C reduces and this makes the diode Ds conduct. The base to collector voltage reduces to 0.4V, which is less the cut- in-voltage of a silicon base-collector junction. Therefore, the transistor does not get saturated.

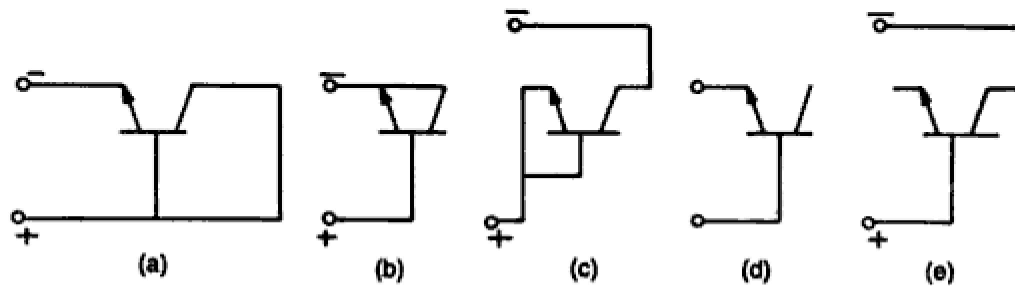
Monolithic diodes:

The diode used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector –base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

Characteristic	(a) $V_{CB} = 0$	(b) $V_{CE} = 0$	(c) $V_{EB} = 0$	(d) $I_C = 0$	(e) $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95



Integrated Resistors:

A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are 1. Diffused 2. epitaxial 3. Pinched and 4. Thin film techniques.

Diffused Resistor:

The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The N-type emitter diffusion and P-type base diffusion are commonly used to realize the monolithic resistor.

The diffused resistor has a severe limitation in that, only small valued resistors can be fabricated. The surface geometry such as the length, width and the diffused impurity profile determine the resistance value. The commonly used parameter for defining this resistance is called the sheet resistance. It is defined as the resistance in ohms/square offered by the diffused area.

In the monolithic resistor, the resistance value is expressed by

$R = R_s\, 1/w$ where R= resistance offered (in ohms)

R_s = sheet resistance of the particular fabrication process involved (in ohms/square)
l = length of the diffused area and

w = width of the diffused area.

The sheet resistance of the base and emitter diffusion in 200Ω/Square and 2.2Ω/square respectively. For example, an emitter-diffused strip of 2mil wide and 20 mil long will offer a resistance of 22Ω. For higher values of resistance, the diffusion region can be formed in a zig-zag fashion resulting in larger effective length. The poly silicon layer can also be used for resistor realization.

Epitaxial Resistor:

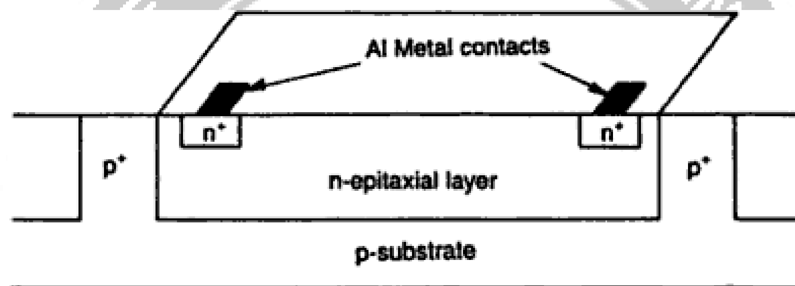


Fig. 1.23 (a) Epitaxial resistor

The N-epitaxial layer can be used for realizing large resistance values. The figure shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two N^+ aluminium metal contacts.

Pinched resistor:

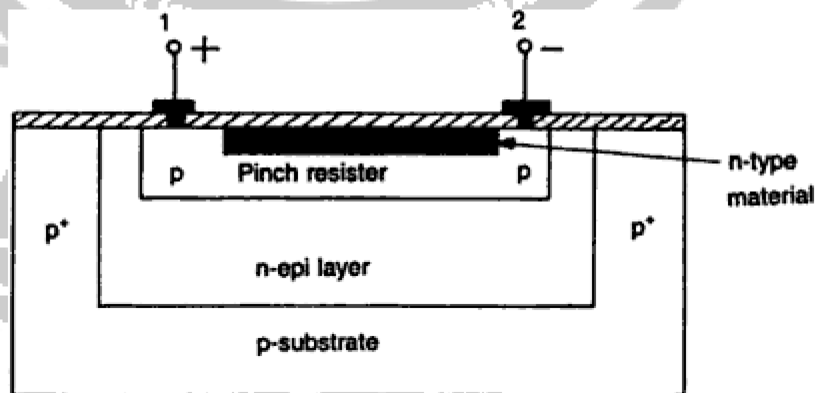


Fig. 1.23 (b) Cross-sectional view of a pinch resistor

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a

comparatively smaller area. In the structure shown, no current can flow in the N-type material since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the wid th narrows down and hence it acts as a pinched resistor.

Thin film resistor:

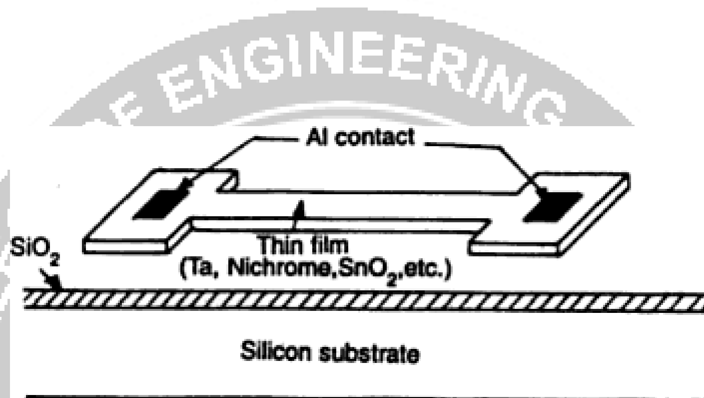


Fig. 1.23 (c) Cross-section of a thin film resistor

The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than 1µm is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome (NiCr) is used for this process. Desired geometry is achieved using masked etching processes to obtain suitable value of resistors. Ohmic contacts are made using aluminium metallization as discussed in earlier sections.

The cross-sectional view of a thin film resistor as shown in figure. Sheet resistances of 40 to 400Ω/ square can be easily obtained in this method and thus 20kΩ to 50kΩ values are very practical.

The advantages of thin film resistors are as follows:

1. They have smaller parasitic components which makes their high frequency behavior good.
2. The thin film resistor values can be very minutely controlled using laser trimming.
3. They have low temperature coefficient of resistance and this makes them more stable.

The thin film resistor can be obtained by the use of tantalum deposited over silicon dioxide layer. The main disadvantage of thin film resistor is that its fabrication requires additional processing steps.

Monolithic Capacitors:

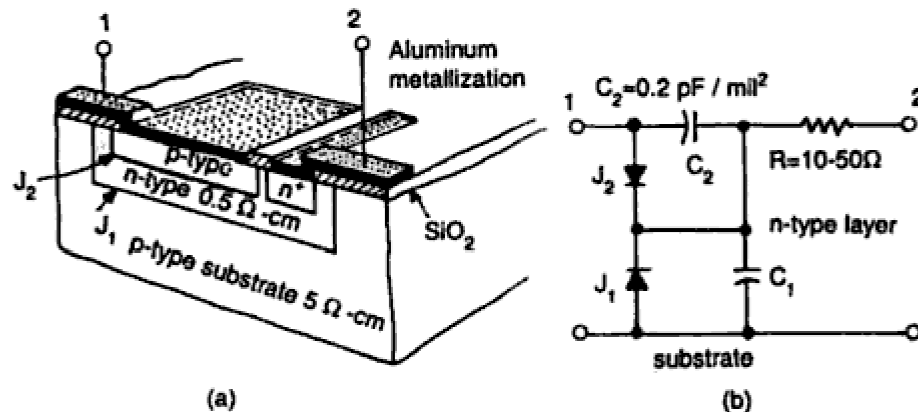


Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor is a reverse biased PN junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

C α A, where a is the area of the junction and

C α T , where t is the thickness of the depletion layer.

The capacitance value thus obtainable can be around $1.2nF/mm^2$.

The thin film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between 0.3 and $0.8nF/mm^2$.

Inductors:

No satisfactory integrated inductors exist. If high Q inductors with inductance of values larger than 5µH are required, they are usually supplied by a wound inductor which is connected externally to the chip. Therefore, the use of inductors is normally avoided when integrated circuits are used.